KSZ8567R

7-Port 10/100 Ethernet Switch with Audio Video Bridging and Two RGMII/MII/RMII Interfaces

Highlights

- Non-blocking wire-speed Ethernet switching fabric
- Full-featured forwarding and filtering control, including Access Control List (ACL) filtering
- Full VLAN and QoS support
- Five ports with integrated 10/100BASE-T PHY transceivers with optional Quiet-WIRE® EMC filtering
- Two ports with 10/100/1000 Ethernet MACs and configurable RGMII/MII/RMII interfaces
- IEEE 1588v2 Precision Time Protocol (PTP) support
- IEEE 802.1AS/Qav Audio Video Bridging (AVB)
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- IEEE 802.1X access control support
- EtherGreen™ power management features, including low power standby
- Flexible management interface options: SPI, I^2C, MIIM, and in-band management via any port
- Industrial/Extended temperature range support
- 128-pin TQFP-EP (14 x 14mm) RoHS compliant pkg

Target Applications

- Industrial Ethernet (Profinet, MODBUS, Ethernet/IP)
- Real-time Ethernet networks
- IEC 61850 networks w/ power substation automation
- Industrial control/automation switches
- Networked measurement and control systems
- Test and measurement equipment

Features

- Switch Management Capabilities
  - 10/100Mbps Ethernet switch basic functions: frame buffer management, address look-up table, queue management, MIB counters
  - Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 4096 entry forwarding table with 256kByte frame buffer
  - Jumbo packet support up to 9000 bytes
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
  - Rapid spanning tree protocol (RSTP) support for topology management and ring/linear recovery
  - Multiple spanning tree protocol (MSTP) support
- Two Configurable External MAC Ports
  - Reduced Gigabit Media Independent Interface (RGMII) v2.0
  - Reduced Media Independent Interface (RMII) v1.2 with 50MHz reference clock input/output option
  - Media Independent Interface (MII) in PHY/MAC mode
- Five Integrated PHY Ports
  - 100BASE-TX/10BASE-T/Te IEEE 802.3
  - Fast Link-up option significantly reduces link-up time
  - Auto-negotiation and Auto-MDI/MDI-X support
  - Energy-Efficient Ethernet (EEE) support with low-power idle mode and clock stoppage
  - On-chip termination resistors and internal biasing for differential pairs to reduce power
  - LinkMD® cable diagnostic capabilities for determining cable opens, shorts, and length
- Advanced Switch Capabilities
  - IEEE 802.1Q VLAN support for 128 active VLAN groups and the full range of 4096 VLAN IDs
  - IEEE 802.1p/Q tag insertion/removal on per port basis
  - VLAN ID on per port or VLAN basis
  - IEEE 802.3x full-duplex flow control and half-duplex back pressure collision control
  - IEEE 802.1X access control (Port and MAC address)
  - IGMP v1/v2/v3 snooping for multicast packet filtering
  - IPv6 multicast listener discovery (MLD) snooping
  - IPv4/IPv6 QoS support, QoS/CoS packet prioritization
  - 802.1p QoS packet classification with 4 priority queues
  - Programmable rate limiting at ingress/egress ports
- IEEE 1588v2 PTP and Clock Synchronization
  - Transparent Clock (TC) with auto correction update
  - Master and slave Ordinary Clock (OC) support
  - End-to-end (E2E) or peer-to-peer (P2P)
  - PTP multicast and unicast message support
  - PTP message transport over IPv4/v6 and IEEE 802.3
  - IEEE 1588v2 PTP packet filtering
  - Synchronous Ethernet support via recovered clock
- Audio Video Bridging (AVB)
  - Compliant with IEEE 802.1BA/AS/Qat/Qav standards
  - Priority queuing, Low latency cut-through mode
  - gPTP time synchronization, credit-based traffic shaper
  - Time aware traffic scheduler per port
- Comprehensive Configuration Registers Access
  - High-speed 4-wire SPI (up to 50MHz), I^2C interfaces provide access to all internal registers
  - MII Management (MIIM, MDC/MDIO 2-wire) Interface provides access to all PHY registers
  - In-band management via any of the data ports
  - I/O pin strapping facility to set certain register bits from I/O pins at reset time
- Power Management
  - IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Energy detect power-down mode on cable disconnect
  - Dynamic clock tree control
  - Unused ports can be individually powered down
  - Full-chip software power-down
  - Wake-on-LAN (WoL) standby power mode with PME interrupt output for system wake upon triggered events

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1.0 PREFACE

1.1 Glossary of Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, 3.3V signaling, IEEE 802.3 compliant
10BASE-Te	10 Mbps Ethernet, 2.5V signaling, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE 802.3u compliant
ADC	Analog-to-Digital Converter
AN	Auto-Negotiation
AVB	Audio Video Bridging (IEEE 802.1BA, 802.1AS, 802.1Qat, 802.1Qav)
BLW	Baseline Wander
BPDU	Bridge Protocol Data Unit. Messages which carry the Spanning Tree Protocol information.
Byte	8 bits
CRC	Cyclic Redundancy Check. A common technique for detection data transmission errors. CRC for Ethernet is 32 bits long.
CSR	Control and Status Registers
DA	Destination Address
DWORD	32 bits
EEE	Energy Efficient Ethernet
FCS	Frame Check Sequence. The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FID	Frame or Filter ID. Specifies the frame identifier. Alternately is the filter identifier.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol. Defined by RFC 1112, RFC 2236, and RFC 4604 to establish multicast group membership in IPv4 networks.
IPG	Inter-Packet Gap. A time delay between successive data packets mandated by the network standard for protocol reasons.
Jumbo Packet	A packet larger than the standard Ethernet packet (1518 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc..
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Controller. A functional block responsible for implementing the media access control layer, which is a sublayer of the data link layer.
MDI	Medium Dependent Interface. An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable.
MDIX	Media Independent Interface with Crossover. An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable.
MIB	Management Information Base. The MIB comprises the management portion of network devices. This can include monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
MII	Media Independent Interface. The MII accesses PHY registers as defined in the IEEE 802.3 specification.
MIIM	Media Independent Interface Management
MLD	Multicast Listening Discovery. This protocol is defined by RFC 3810 and RFC 4604 to establish multicast group membership in IPv6 networks.
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZ	Non Return to Zero. A type of signal data encoding whereby the signal does not return to a zero state in between bits.
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
PHY	A device or function block which performs the physical layer interface function in a network.
PLL	Phase Locked Loop. A electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal.
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter. The 8-bit value indicating the end of the preamble of an Ethernet frame.
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
TCP	Transmission Control Protocol
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UTP	Unshielded Twisted Pair. Commonly a cable containing 4 twisted pairs of wire.
UUID	Universally Unique IDentifier
VLAN	Virtual Local Area Network
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input
IPU	Input with internal pull-up (58 kΩ ±30%)
IPU/O	Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin during normal operation
IPD	Input with internal pull-down (58 kΩ ±30%)
IPD/O	Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin during normal operation
O8	Output with 8 mA sink and 8 mA source
O24	Output with 24 mA sink and 24 mA source
OPU	Output (8mA) with internal pull-up (58 kΩ ±30%)
OPD	Output (8mA) with internal pull-down (58 kΩ ±30%)
A	Analog
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power
GND	Ground

Note: Refer to Section 6.3, "Electrical Characteristics," on page 198 for the electrical characteristics of the various buffers.

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
LL	**Latch Low:** Applies to certain RO status bits. If a status condition causes this bit to go low, it will maintain the low state until read, even if the status condition changes. A read clears the latch, allowing the bit to go high if dictated by the status condition.
LH	**Latch High:** Applies to certain RO status bits. If a status condition causes this bit to go high, it will maintain the high state until read, even if the status condition changes. A read clears the latch, allowing the bit to go low if dictated by the status condition.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

1.4 References

- NXP I^2C-Bus Specification (UM10204, April 4, 2014): www.nxp.com/documents/user_manual/UM10204.pdf

2.0 INTRODUCTION

2.1 General Description

The KSZ8567R is a highly-integrated, IEEE 802.3 compliant networking device that incorporates a layer-2 managed high-performance Ethernet switch, five 10BASE-T/Te/100BASE-TX physical layer transceivers (PHYs) and associated MAC units, and two MAC ports with individually configurable RGMII/MII/RMII interfaces for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver.

The KSZ8567R is built upon industry-leading Ethernet technology, with features designed to offload host processing and streamline the overall design:

- Non-blocking wire-speed Ethernet switch fabric
- Full-featured forwarding and filtering control, including port-based Access Control List (ACL) filtering
- Full VLAN and QoS support
- Traffic prioritization with per-port ingress/egress queues and by traffic classification
- Spanning Tree support
- IEEE 802.1X access control support

The KSZ8567R incorporates full hardware support for the IEEE 1588v2 Precision Time Protocol (PTP), including hardware time-stamping at all PHY-MAC interfaces, and a high-resolution hardware “PTP clock”. IEEE 1588 provides sub-microsecond synchronization for a range of industrial Ethernet applications.

The KSZ8567R fully supports the IEEE family of Audio Video Bridging (AVB) standards, which provides high Quality of Service (QoS) for latency sensitive traffic streams over Ethernet. Time-stamping and time-keeping features support IEEE 802.1AS time synchronization. All ports feature credit based traffic shapers for IEEE 802.1Qav, and a time aware scheduler as proposed for IEEE 802.1Qbv.

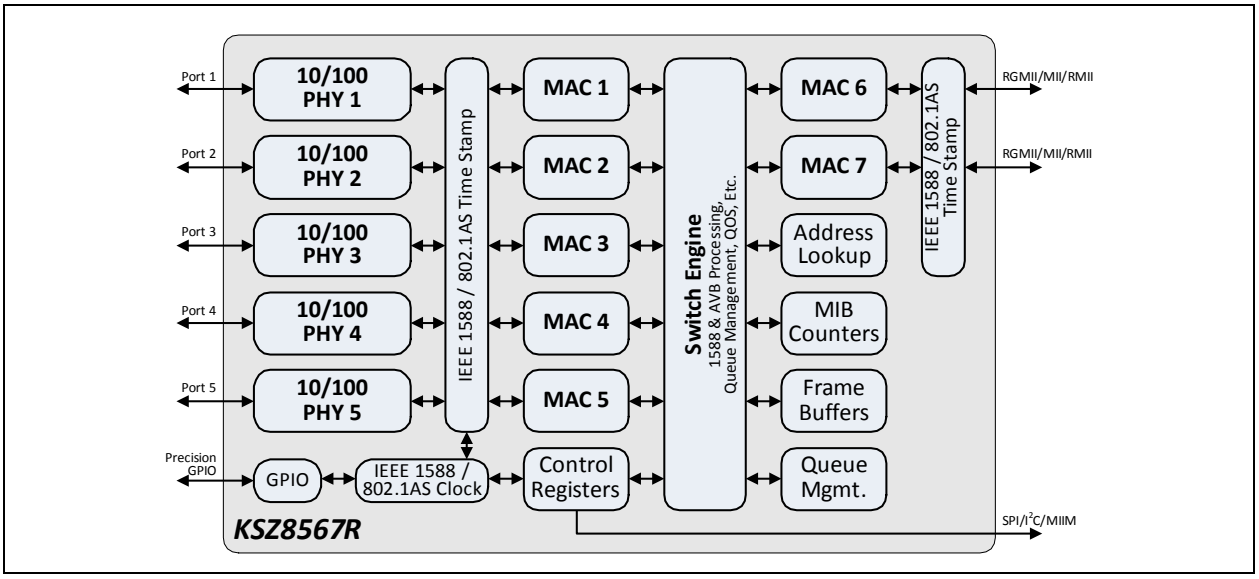
The 100Mbps PHYs feature Quiet-WIRE internal filtering to reduce line emissions and enhance immunity to environmental noise. It is ideal for automotive or industrial applications where stringent radiated emission limits must be met.

A host processor can access all KSZ8567R registers for control over all PHY, MAC, and switch functions. Full register access is available via the integrated SPI or I^2C interfaces, and by in-band management via any one of the data ports. PHY register access is provided by a MIIM interface. Flexible digital I/O voltage allows the MAC port to interface directly with a 1.8/2.5/3.3V host processor/controller/FPGA.

Additionally, a robust assortment of power-management features including IEEE 802.3az Energy-Efficient Ethernet (EEE) for power savings with idle link, and Wake-on-LAN (WoL) for low power standby operation, have been designed to satisfy energy-efficient system requirements.

The KSZ8567R is available in industrial (-40°C to +85°C) and extended (-40°C to +105°C) temperature ranges. An internal block diagram of the KSZ8567R is shown in Figure 2-1.

FIGURE 2-1: INTERNAL BLOCK DIAGRAM

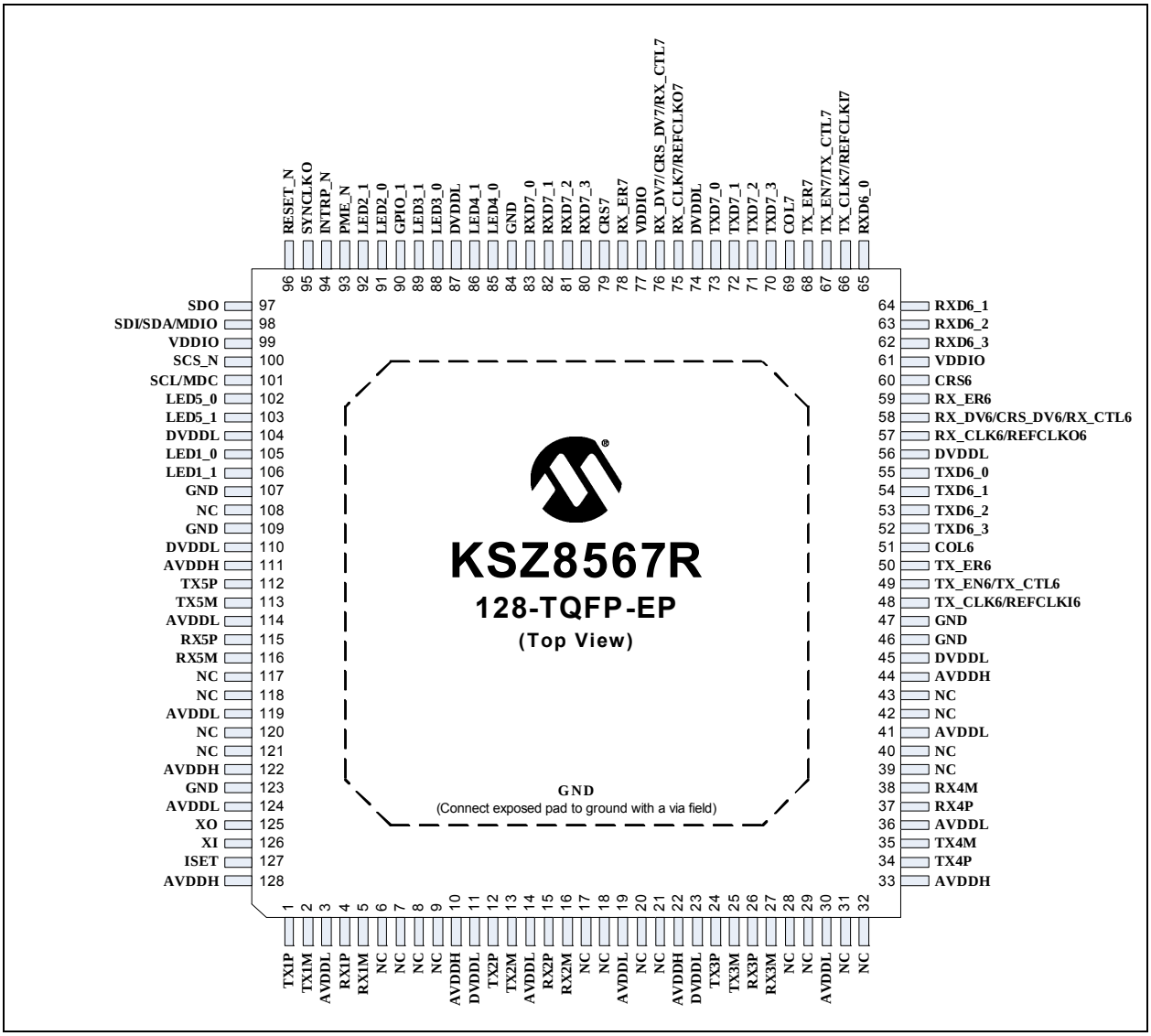


3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

The device pin diagram for the KSZ8567R can be seen in Figure 3-1. Table 3-1 provides a KSZ8567R pin assignment table. Pin descriptions are provided in Section 3.2, "Pin Descriptions".

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: When an "_N" is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.2, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

TABLE 3-1: PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	TX1P	33	AVDDH	65	RXD6_0 (Note 3-1)	97	SDO
2	TX1M	34	TX4P	66	TX_CLK7/REFCLKI7	98	SDI/SDA/MDIO
3	AVDDL	35	TX4M	67	TX_EN7/TX_CTL7	99	VDDIO
4	RX1P	36	AVDDL	68	TX_ER7	100	SCS_N
5	RX1M	37	RX4P	69	COL7	101	SCL/MDC
6	NC	38	RX4M	70	TXD7_3	102	LED5_0
7	NC	39	NC	71	TXD7_2	103	LED5_1 (Note 3-1)
8	NC	40	NC	72	TXD7_1	104	DVDDL
9	NC	41	AVDDL	73	TXD7_0	105	LED1_0
10	AVDDH	42	NC	74	DVDDL	106	LED1_1 (Note 3-1)
11	DVDDL	43	NC	75	RX_CLK7/REFCLKO7	107	GND
12	TX2P	44	AVDDH	76	RX_DV7/CRS_DV7/ RX_CTL7 (Note 3-1)	108	NC
13	TX2M	45	DVDDL	77	VDDIO	109	GND
14	AVDDL	46	GND	78	RX_ER7	110	DVDDL
15	RX2P	47	GND	79	CRS7	111	AVDDH
16	RX2M	48	TX_CLK6/REFCLKI6	80	RXD7_3 (Note 3-1)	112	TX5P
17	NC	49	TX_EN6/TX_CTL6	81	RXD7_2 (Note 3-1)	113	TX5M
18	NC	50	TX_ER6	82	RXD7_1 (Note 3-1)	114	AVDDL
19	AVDDL	51	COL6	83	RXD7_0 (Note 3-1)	115	RX5P
20	NC	52	TXD6_3	84	GND	116	RX5M
21	NC	53	TXD6_2	85	LED4_0 (Note 3-1)	117	NC
22	AVDDH	54	TXD6_1	86	LED4_1 (Note 3-1)	118	NC
23	DVDDL	55	TXD6_0	87	DVDDL	119	AVDDL
24	TX3P	56	DVDDL	88	LED3_0	120	NC
25	TX3M	57	RX_CLK6/REFCLKO6	89	LED3_1 (Note 3-1)	121	NC
26	RX3P	58	RX_DV6/CRS_DV6/ RX_CTL6	90	GPIO_1	122	AVDDH
27	RX3M	59	RX_ER6	91	LED2_0 (Note 3-1)	123	GND
28	NC	60	CRS6	92	LED2_1 (Note 3-1)	124	AVDDL
29	NC	61	VDDIO	93	PME_N	125	XO
30	AVDDL	62	RXD6_3 (Note 3-1)	94	INTRP_N	126	XI
31	NC	63	RXD6_2 (Note 3-1)	95	SYNCLKO	127	ISET
32	NC	64	RXD6_1 (Note 3-1)	96	RESET_N	128	AVDDH
Exposed Pad Must be Connected to GND							

Note 3-1 This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.

3.2 Pin Descriptions

This sections details the functions of the various device signals.

TABLE 3-2: PIN DESCRIPTIONS

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Ports 5-1 10/100 Ethernet Pins			
Port 5-1 Ethernet TX +	**TX[5:1]P**	AIO	Port 5-1 100BASE-TX/10BASE-T Differential Data (+) Transmit when in MDI mode, receive when in MDI-X mode.
Port 5-1 Ethernet TX -	**TX[5:1]M**	AIO	Port 5-1 100BASE-TX/10BASE-T Differential Data (-) Transmit when in MDI mode, receive when in MDI-X mode.
Port 5-1 Ethernet RX +	**RX[5:1]P**	AIO	Port 5-1 100BASE-TX/10BASE-T Differential Data (+) Receive when in MDI mode, transmit when in MDI-X mode.
Port 5-1 Ethernet RX -	**RX[5:1]M**	AIO	Port 5-1 100BASE-TX/10BASE-T Differential Data (-) Receive when in MDI mode, transmit when in MDI-X mode.
Ports 7-6 RGMII/MII/RMII Pins			
Port 7-6 Transmit/ Reference Clock	**TX_CLK[7:6]/ REFCLKI[7:6]**	I/O8	**MII Mode:** **TX_CLK[7:6]** is the Port 7-6 25/2.5MHz Transmit Clock. In PHY mode this pin is an output, in MAC mode it is an input. **RMII Mode:** **REFCLKI[7:6]** is the Port 7-6 50MHz Reference Clock input when in RMII Normal mode. This pin is unused when in RMII Clock mode. **RGMII Mode:** **TX_CLK[7:6]** is the Port 7-6 125/25/2.5MHz Transmit Clock input.
Port 7-6 Transmit Enable/Control	**TX_EN[7:6]/ TX_CTL[7:6]**	IPD	**MII/RMII Modes:** **TX_EN[7:6]** is the Port 7-6 Transmit Enable. **RGMII Mode:** **TX_CTL[7:6]** is the Port 7-6 Transmit Control.
Port 7-6 Transmit Error	**TX_ER[7:6]**	IPD	**MII Mode:** Port 7-6 Transmit Error input. **RMII/RGMII Modes:** Not used. Do not connect this pin in these modes of operation.
Port 7-6 Collision Detect	**COL[7:6]**	IPD/O8	**MII Mode:** Port 7-6 Collision Detect. In PHY mode this pin is an output, in MAC mode it is an input. **RMII/RGMII Modes:** Not used. Do not connect this pin in these modes of operation.
Port 7-6 Transmit Data 3	**TXD[7:6]_3**	IPD	**MII/RGMII Modes:** Port 7-6 Transmit Data bus bit 3. **RMII Mode:** Not used. Do not connect this pin in this mode of operation.
Port 7-6 Transmit Data 2	**TXD[7:6]_2**	IPD	**MII/RGMII Modes:** Port 7-6 Transmit Data bus bit 2. **RMII Mode:** Not used. Do not connect this pin in this mode of operation.
Port 7-6 Transmit Data 1	**TXD[7:6]_1**	IPD	**MII/RMII/RGMII Modes:** Port 7-6 Transmit Data bus bit 1.
Port 7-6 Transmit Data 0	**TXD[7:6]_0**	IPD	**MII/RMII/RGMII Modes:** Port 7-6 Transmit Data bus bit 0.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Port 7-6 Receive/ Reference Clock	**RX_CLK[7:6]/ REFCLKO[7:6]**	I/O24	**MII Mode: RX_CLK[7:6]** is the Port 7-6 25/2.5MHz Receive Clock. In PHY mode this pin is an output, in MAC mode it is an input. **RMII Mode: REFCLKO[7:6]** is the Port 7-6 50MHz Reference Clock output when in RMII Clock mode. This pin is unused when in RMII Normal mode. **RGMII Mode: RX_CLK[7:6]** is the Port 7-6 125/25/2.5MHz Receive Clock output.
Port 7-6 Receive Data Valid / Carrier Sense / Control	**RX_DV[7:6]/ CRS_DV[7:6]/ RX_CTL[7:6]**	IPD/O24	**MII Mode: RX_DV[7:6]** is the Port 7-6 Received Data Valid output. **RMII Mode: CRS_DV[7:6]** is the Carrier Sense / Receive Data Valid output. **RGMII Mode: RX_CTL[7:6]** is the Receive Control output. **Note:** The **RX_DV7/CRS_DV7/RX_CTL7** pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 7-6 Receive Error	**RX_ER[7:6]**	IPD/O24	**MII Mode:** Port 7-6 Receive Error output. **RMII/RGMII Modes:** Not used. Do not connect this pin in these modes of operation.
Port 7-6 Carrier Sense	**CRS[7:6]**	IPD/O8	**MII Mode:** Port 7-6 Carrier Sense. In PHY mode this pin is an output, in MAC mode it is an input. **RMII/RGMII Modes:** Not used. Do not connect this pin in these modes of operation.
Port 7-6 Receive Data 3	**RXD[7:6]_3**	IPD/O24	**MII/RGMII Modes:** Port 7-6 Receive Data bus bit 3. **RMII Mode:** Not used. Do not connect this pin in this mode of operation. **Note:** These pins also provide configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 7-6 Receive Data 2	**RXD[7:6]_2**	IPD/O24	**MII/RGMII Modes:** Port 7-6 Receive Data bus bit 2. **RMII Mode:** Not used. Do not connect this pin in this mode of operation. **Note:** These pins also provide configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 7-6 Receive Data 1	**RXD[7:6]_1**	IPD/O24	**MII/RMII/RGMII Modes:** Port 7-6 Receive Data bus bit 1. **Note:** These pins also provide configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Port 7-6 Receive Data 0	**RXD[7:6]_0**	IPD/O24	**MII/RMII/RGMII Modes:** Port 7-6 Receive Data bus bit 0. **Note:** These pins also provide configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
SPI/I²C/MIIM Interface Pins			
SPI/I²C/MIIM Serial Clock	**SCL/MDC**	IPU	**SPI/I²C Modes:** **SCL** serial clock. **MIIM Mode:** **MDC** serial clock.
SPI Data Out	**SDO**	O8	**SPI Mode:** Data out (also known as MISO). **I²C/MIIM Modes:** Not used.
SPI Data In / I²C/MIIM Data In/Out	**SDI/SDA/MDIO**	IPU/O8	**SPI Mode:** **SDI** Data In (also known as MOSI). **I²C Mode:** **SDA** Data In/Out. **MIIM Mode:** **MDIO** Data In/Out. **SDI** and **MDIO** are open-drain signals when in the output state. An external pull-up resistor to **VDDIO** (1.0kΩ to 4.7kΩ) is required.
SPI Chip Select	**SCS_N**	IPU	**SPI Mode:** Chip Select (active low). **I²C/MIIM Modes:** Not used.
LED Pins			
Port 1 LED Indicator 0	**LED1_0**	IPU/O8	Port 1 LED Indicator 0. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 1 LED Indicator 1	**LED1_1**	IPU/O8	Port 1 LED Indicator 1. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 2 LED Indicator 0	**LED2_0**	IPU/O8	Port 2 LED Indicator 0. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 2 LED Indicator 1	**LED2_1**	IPU/O8	Port 2 LED Indicator 1. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Port 3 LED Indicator 0	**LED3_0**	IPU/O8	Port 3 LED Indicator 0. Active low output sinks current to light an external LED.
Port 3 LED Indicator 1	**LED3_1**	IPU/O8	Port 3 LED Indicator 1. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 4 LED Indicator 0	**LED4_0**	IPU/O8	Port 4 LED Indicator 0. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 4 LED Indicator 1	**LED4_1**	IPU/O8	Port 4 LED Indicator 1. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 5 LED Indicator 0	**LED5_0**	IPU/O8	Port 5 LED Indicator 0. Active low output sinks current to light an external LED.
Port 5 LED Indicator 1	**LED5_1**	IPU/O8	Port 5 LED Indicator 1. Active low output sinks current to light an external LED. **Note:** This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Miscellaneous Pins			
Interrupt	**INTRP_N**	OPU	Active low, open-drain interrupt. **Note:** This pin requires an external pull-up resistor.
Power Management Event	**PME_N**	O8	Power Management Event. This output signal indicates that an energy detect event has occurred. It is intended to wake up the system from a low power mode. **Note:** The assertion polarity is programmable (default active low). An external pull-up resistor is required for active-low operation; an external pull-down resistor is required for active-high operation.
System Reset	**RESET_N**	IPU	Active low system reset. The device must be reset either during or after power-on. An RC circuit is suggested for power-on reset.
Crystal Clock / Oscillator Input	**XI**	ICLK	Crystal clock / oscillator input. When using a 25MHz crystal, this input is connected to one lead of the crystal. When using an oscillator, this pin is the input from the oscillator. The crystal oscillator should have a tolerance of ±50ppm.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Crystal Clock Output	**XO**	OCLK	Crystal clock / oscillator output. When using a 25MHz crystal, this output is connected to one lead of the crystal. When using an oscillator, this pin is left unconnected.
25/125MHz Reference Clock Output	**SYNCLKO**	O24	25/125MHz reference clock output, derived from the crystal input or the recovered clock of any PHY. This signal may be used for Synchronous Ethernet.
General Purpose Input/Output 1	**GPIO_1**	IPU/O8	This signal can be used as an input or output for use by the IEEE 1588 event trigger or timestamp capture units. It will be synchronized to the internal IEEE 1588 clock. This pin can also be controlled (as an output) or sampled (as an input) via device registers.
Transmit Output Current Set Resistor	**ISET**	A	Transmit output current set resistor. This pin configures the physical transmit output current. It must be connected to **GND** through a 6.04kΩ 1% resistor.
No Connect	**NC**	-	No Connect. For proper operation, this pin must be left unconnected.
Power/Ground Pins			
+3.3/2.5/1.8V I/O Power	**VDDIO**	P	+3.3V / +2.5V / +1.8V I/O Power
+3.3/2.5V Analog Power	**AVDDH**	P	+3.3V / +2.5V Analog Power
+1.2V Analog Power	**AVDDL**	P	+1.2V Analog Power
+1.2V Digital Power	**DVDDL**	P	+1.2V Digital Power
Ground	**GND**	GND	Ground (pins and pad)

3.2.1 CONFIGURATION STRAPS

The KSZ8567R utilizes configuration strap pins to configure the device for different modes. While **RESET_N** is low, these pins are hi-Z. Pull-up/down resistors are used to create high or low states on these pins, which are internally sampled at the rising edge of **RESET_N**. All of these pins have a weak internal pull-up or pull-down resistor which provides a default level for strapping. To strap an LED pin low, use a 750Ω to 1kΩ external pull-down resistor. To strap a non-LED pin high, use an external 1kΩ to 10kΩ pull-up resistor to **VDDIO**. Once **RESET_N** is high, all of these pins become driven outputs.

Because the internal pull-up/down resistors are not strong, consideration must be given to any other pull-up/down resistors which may reside on the board or inside a device connected to these pins.

When an LED pin is directly driving an LED, the effect of the LED and LED load resistor on the strapping level must be considered. This is the reason for using a small value resistor to pull an LED pin low. This is especially true when an LED is powered from a voltage that is higher than **VDDIO**.

The configuration strap pins and their associated functions are detailed in Table 3-3.

TABLE 3-3: CONFIGURATION STRAP DESCRIPTIONS

CONFIGURATION STRAP PIN	DESCRIPTION
LED1_0	**Quiet-WIRE Filtering Enable** 0: Quiet-WIRE filtering enabled 1: Quiet-WIRE filtering disabled (Default)
LED1_1	**Flow Control (All Ports)** 0: Flow control disabled 1: Flow control enabled (Default)
LED2_1	**Link-up Mode (All PHYs)** 0: Fast Link-up: Auto-negotiation and auto MDI/MDI-X are disabled 1: Normal Link-up: Auto-negotiation and auto MDI/MDI-X are enabled (Default) **Note:** Since Fast Link-up disables auto-negotiation and auto-crossover, it is suitable only for specialized applications.
LED2_0, LED4_0	**When LED2_1 = 1 at strap-in (Normal Link-up):** **[LED2_0, LED4_0]: Auto-Negotiation Enable (All PHYs) / NAND Tree Test Mode** 00: Reserved 01: Auto-negotiation disabled 10: NAND Tree test mode 11: Auto-negotiation enabled (Default) **When LED2_1 = 0 at strap-in (Fast Link-up; All PHYs Full-Duplex):** **LED2_0: MDI/MDI-X Mode (All PHYs)** 0: MDI-X 1: MDI (Default) **LED4_0: Not Used**
LED4_1, LED3_1	**[LED4_1, LED3_1]: Management Interface Mode** 00: MIIM (MDIO) 01: I^2C 1x: SPI (Default)
LED5_1	**Switch Enable at Startup** 0: Start Switch is disabled. The switch will not forward packets until the Start Switch bit is set in the Switch Operation Register. 1: Start Switch is enabled. The switch will forward packets immediately after reset. (Default)
RXD6_3, RXD6_2	**[RXD6_3, RXD6_2]: Port 6 Mode** 00: RGMII (Default) 01: RMII 10: Reserved 11: MII

TABLE 3-3: CONFIGURATION STRAP DESCRIPTIONS (CONTINUED)

CONFIGURATION STRAP PIN	DESCRIPTION
RXD6_1	**Port 6 MII/RMII Mode** 0: MII: PHY Mode (Default) RMII: Clock Mode. RMII 50MHz reference clock is output on **REFCLKO6**. (Default) RGMII: No effect 1: MII: MAC Mode RMII: Normal Mode. RMII 50MHz reference clock is input on **REFCLKI6**. RGMII: No effect
RXD6_0	**Port 6 Speed Select** 0: 1000Mbps Mode (Default) 1: 10/100Mbps Mode **Note:** If Port 6 is configured for MII or RMII, set the speed to 100Mbps.
RXD7_3, RXD7_2	**[RXD7_3, RXD7_2]: Port 7 Mode** 00: RGMII (Default) 01: RMII 10: Reserved 11: MII
RXD7_1	**Port 7 MII/RMII Mode** 0: MII: PHY Mode (Default) RMII: Clock Mode. RMII 50MHz reference clock is output on **REFCLKO7**. (Default) RGMII: No effect 1: MII: MAC Mode RMII: Normal Mode. RMII 50MHz reference clock is input on **REFCLKI7**. RGMII: No effect
RXD7_0	**Port 7 Speed Select** 0: 1000Mbps Mode (Default) 1: 10/100Mbps Mode **Note:** If Port 7 is configured for MII or RMII, set the speed to 100Mbps.
RX_DV7/CRS_DV7/ RX_CTL7	**In-Band Management** 0: Disable In-Band Management (Default) 1: Enable In-Band Management

4.0 FUNCTIONAL DESCRIPTION

This section provides functional descriptions for the following:

- Physical Layer Transceiver (PHY)
- LEDs
- Media Access Controller (MAC)
- Switch
- IEEE 1588 Precision Time Protocol
- Audio Video Bridging and Time Sensitive Networks
- NAND Tree Support
- Clocking
- Power
- Power Management
- Management Interface
- In-Band Management
- MAC Interface (RGMII/MII/RMII Port 6-7)

4.1 Physical Layer Transceiver (PHY)

Ports 1 through 5 include completely integrated dual-speed (10BASE-T/Te, 100BASE-TX) Ethernet physical layer transceivers for transmission and reception of data over standard four-pair unshielded twisted pair (UTP), CAT-5 or better Ethernet cable. At 100Mbps, the optional Quiet-WIRE filtering feature reduced emissions while maintaining interoperability with standard 100BASE-TX devices.

The device reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs, eliminating the need for external termination resistors. The internal chip termination and biasing provides significant power savings when compared with using external biasing and termination resistors.

4.1.1 100BASE-TX TRANSCEIVER

4.1.1.1 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external ISET resistor sets the output current for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T/Te output driver is also incorporated into the 100BASE-TX driver.

4.1.1.2 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

4.1.1.3 Scrambler/De-Scrambler

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. The scrambler is used only for 100BASE-TX.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

4.1.2 10BASE-T/Te TRANSCEIVER

When the **AVDDH** supply is 3.3V, the 10Mbps interface is 10BASE-T. When **AVDDH** is 2.5V, the 10BASE-T signal has a reduced transmit signal amplitude and is known as 10BASE-Te. 10BASE-Te is interoperable to 100m with 10BASE-T when Cat5 cable is used.

4.1.2.1 10BASE-T/Te Transmit

The 10BASE-T/Te driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.5V amplitude for 10BASE-T, or 1.75V amplitude for 10BASE-Te. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

4.1.2.2 10BASE-T/Te Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the device decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

4.1.3 AUTO MDI/MDI-X

The automatic MDI/MDI-X feature, also known as auto crossover, eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. The auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the device accordingly. Table 4-1 shows the device's 10/100 Mbps pin configuration assignments for MDI and MDI-X pin mapping.

TABLE 4-1: MDI/MDI-X PIN DEFINITIONS

Pin (RJ45 pair)	MDI		MDI-X	
	100BASE-TX	10BASE-T/Te	100BASE-TX	10BASE-T/Te
TXP/M_A (1,2)	TX+/-	TX+/-	RX+/-	RX+/-
RXP/M_A (3,6)	RX+/-	RX+/-	TX+/-	TX+/-

Auto MDI/MDI-X is enabled by default. It can be disabled through the port control registers. If Auto MDI/MDI-X is disabled, the port control register can also be used to select between MDI and MDI-X settings.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

4.1.4 WAVE SHAPING, SLEW-RATE CONTROL, AND PARTIAL RESPONSE

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T/Te, pre-emphasis is used to extend the signal quality through the cable.

4.1.5 AUTO-NEGOTIATION

The device conforms to the auto-negotiation protocol as described by IEEE 802.3. Auto-negotiation allows each port to operate at either 10BASE-T/Te or 100BASE-TX by allowing link partners to select the best common mode of operation. During auto-negotiation, the link partners advertise capabilities across the link to each other and then compare their own

capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is also used to negotiate support for Energy Efficient Ethernet (EEE) via the next page feature.

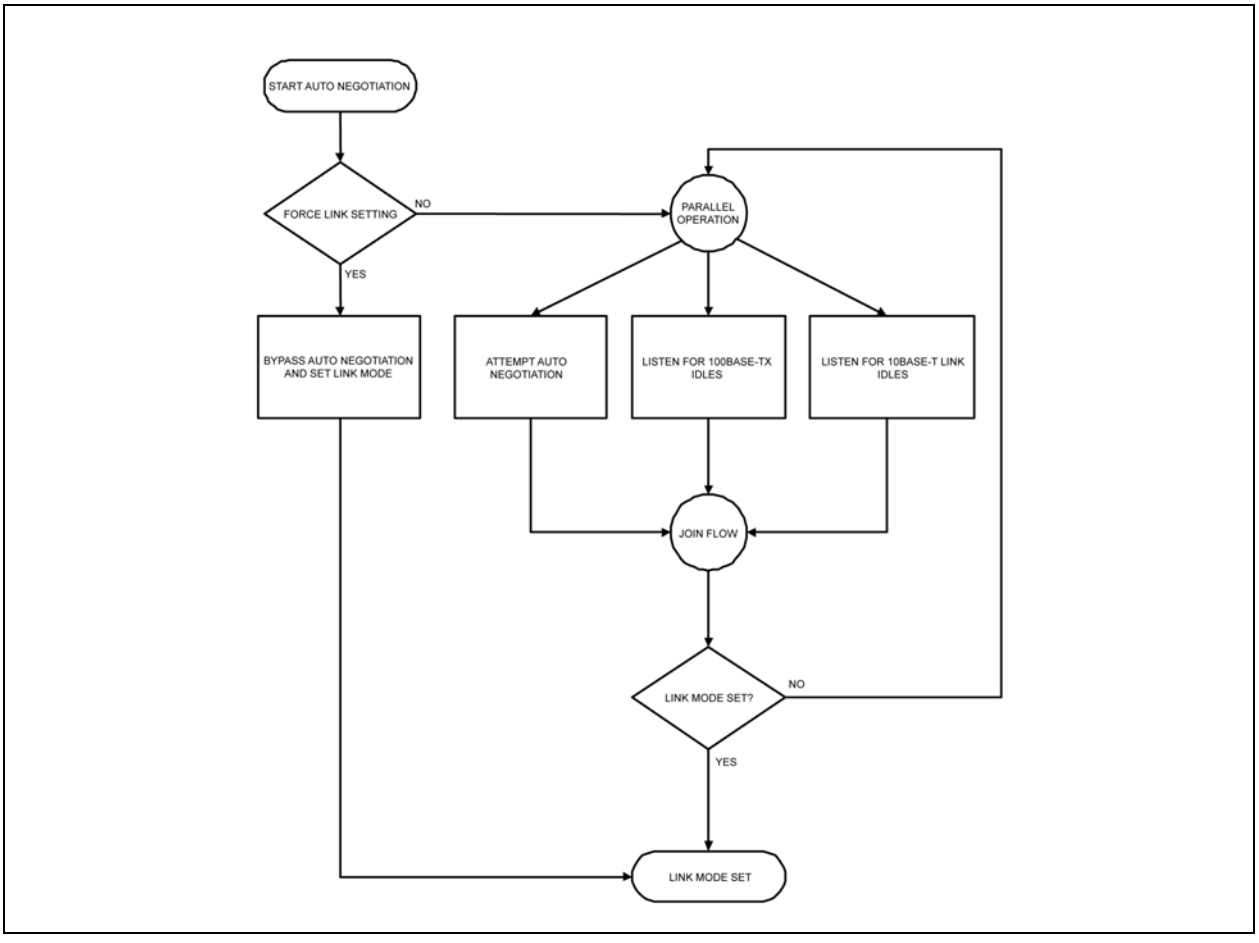
The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T/Te, full-duplex
- Priority 4: 10BASE-T/Te, half-duplex

If the KSZ8567R link partner doesn't support auto-negotiation or is forced to bypass auto-negotiation, the KSZ8567R port sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8567R to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 4-1.

FIGURE 4-1: AUTO-NEGOTIATION AND PARALLEL OPERATION



Auto-negotiation is enabled by default after power-up or hardware reset. Afterwards, auto-negotiation can be enabled or disabled via bit 12 of the PHY Basic Control Register. If auto-negotiation is disabled, the speed is set by bit 13 of the PHY Basic Control Register, and the duplex is set by bit 8.

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection initiate until a common speed between the KSZ8567R and its link partner is re-established for a link.

If link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through bit 9 of the PHY Basic Control Register, or a link-down to link-up transition occurs (i.e. disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the PHY Basic Status Register, and the link partner capabilities are updated in the PHY Auto-Negotiation Link Partner Ability Register and PHY Auto-Negotiation Expansion Status Register.

4.1.6 QUIET-WIRE FILTERING

Quiet-WIRE is a feature to enhance 100BASE-TX EMC performance by reducing both conducted and radiated emissions from the TXP/M signal pair. It can be used either to reduce absolute emissions, or to enable replacement of shielded cable with unshielded cable, all while maintaining interoperability with standard 100BASE-TX devices.

Quiet-WIRE filtering is implemented internally, with no additional external components required. It is enabled or disabled for all PHYs at power-up and reset by a strapping option on the **LED1_0** pin. Once the device is powered up, Quiet-WIRE can be enabled or disabled by writing to the appropriate control register.

The default setting for Quiet-WIRE reduces emissions primarily above 60MHz, with less reduction at lower frequencies. Several dB of reduction is possible. Signal attenuation is approximately equivalent to increasing the cable length by 10 to 20 meters, thus reducing cable reach by that amount. For applications needing more modest improvement in emissions, the level of filtering can be reduced by writing to certain registers.

4.1.7 FAST LINK-UP

Link up time is normally determined by the time it takes to complete auto-negotiation. Additional time may be added by the auto MDI/MDI-X feature. The total link up time from power-up or cable connect is typically a second or more.

Fast Link-up mode significantly reduces 100BASE-TX link-up time by disabling both auto-negotiation and auto MDI/MDI-X, and fixing the TX and RX channels. This mode is enabled or disabled by the **LED2_1** strapping option. It is not set by registers, so fast link-up is available immediately upon power-up. Fast Link-up is available at power-up only for 100BASE-TX link speed, which is selected by strapping the **LED4_0** pin high. Fast Link-up is also available for 10BASE-T/Te, but this link speed must first be selected via a register write.

Fast Link-up is intended for specialized applications where both link partners are known in advance. The link must also be known so that the fixed transmit channel of one device connects to the fixed receive channel of the other device, and vice versa. The TX and RX channel assignments are determined by the MDI/MDI-X strapping option on **LED2_0**.

If a device in Fast Link-up mode is connected to a normal device (auto-negotiate and auto-MDI/MDI-X), there will be no problems linking, but the speed advantage of Fast Link-up will not be realized.

For more information on configuration straps, refer to Section 3.2.1, "Configuration Straps," on page 16.

4.1.8 LinkMD® CABLE DIAGNOSTICS

The LinkMD® function utilizes Time Domain Reflectometry (TDR) to analyze the cabling for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD® function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

4.1.9 LinkMD®+ ENHANCED DIAGNOSTICS: RECEIVE SIGNAL QUALITY INDICATOR

The device provides a receive Signal Quality Indicator (SQI) feature, which indicates the relative quality of the 100BASE-TX receive signal. It approximates a signal-to-noise ratio, and is affected by cable length, cable quality, and coupled of environmental noise.

The raw SQI value is available for reading at any time from the SQI register. A lower value indicates better signal quality, while a higher value indicates worse signal quality. Even in a stable configuration in a low-noise environment, the value read from this register may vary. The value should therefore be averaged by taking multiple readings. The update interval of the SQI register is 2µs, so measurements taken more frequently than 2µs will be redundant. In a quiet environment, 6 to 10 readings are suggested for averaging. In a noisy environment, individual readings are unreliable, so a minimum of 30 readings are suggested for averaging. The SQI circuit does not include any hysteresis.

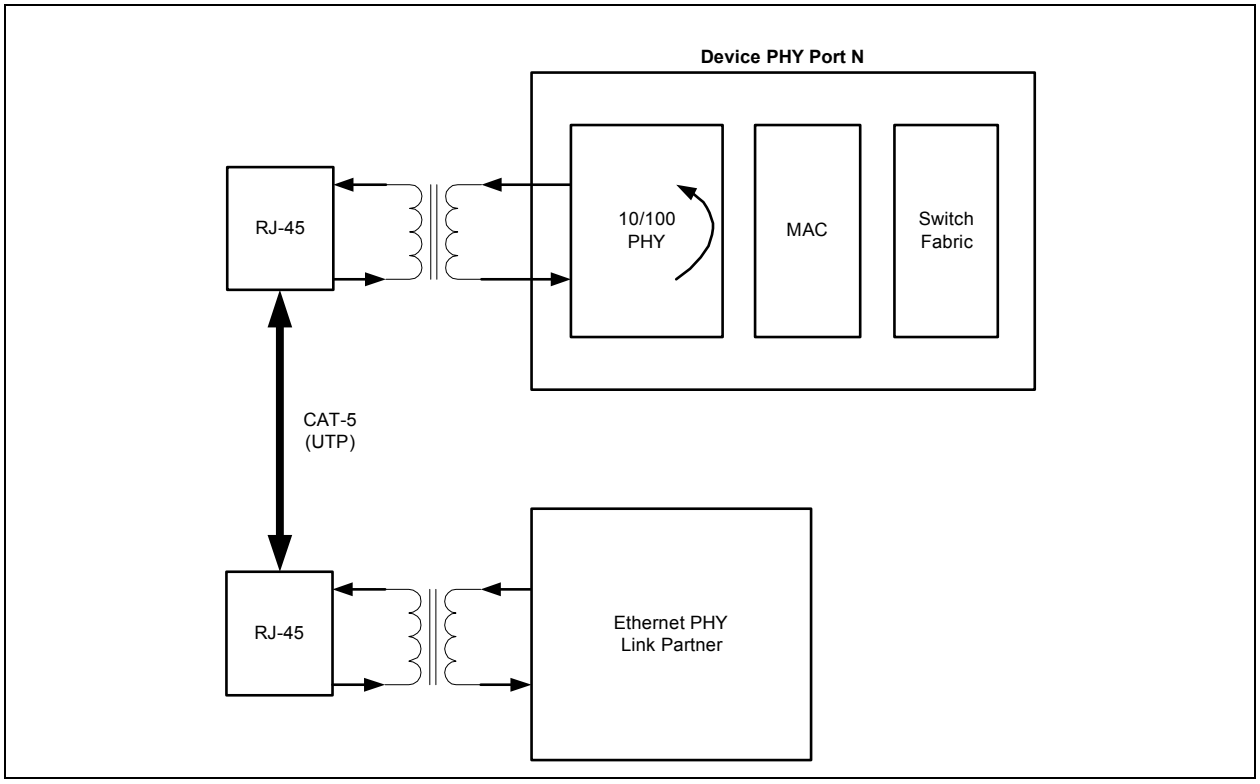
4.1.10 REMOTE PHY LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8567R and its Ethernet PHY link partner, and is supported for 10/100 Mbps at full-duplex.

The loopback data path is shown in Figure 4-2 and functions as follows:

- The Ethernet PHY link partner transmits data to the KSZ8567R PHY port.
- Data received at the external pins of the PHY port is looped back without passing through the MAC and internal switch fabric.
- The same KSZ8567R PHY port transmits data back to the Ethernet PHY link partner.

FIGURE 4-2: REMOTE PHY LOOPBACK



The following programming steps and register settings are for remote PHY loopback mode for 100BASE-TX Mode, and 10BASE-T Mode.

- 100BASE-TX Mode
  - Set Port N (1-5), PHY Auto-Negotiation Advertisement Register = 0x0181
  - Set Port N (1-5), PHY Remote Loopback Register = 0x01F0
  - Set Port N (1-5), PHY Basic Control Register = 0x3300

- 10BASE-T Mode
  - Set Port N (1-5), PHY Auto-Negotiation Advertisement Register = 0x0061
  - Set Port N (1-5), PHY Remote Loopback Register = 0x01F0
  - Set Port N (1-5), PHY Basic Control Register = 0x3300

4.2 LEDs

Each PHY port has two programmable LED output pins, **LED*x*_0** and **LED*x*_1**, to indicate the PHY link and activity status. Two different LED modes are available. The LED mode can be changed individually for each PHY port by writing to the PHY Mode bit in the PHY indirect register: MMD 2, address 0, bit 4:

- 1 = Single-LED Mode
- 0 = Tri-Color Dual-LED Mode (Default)

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω). LED outputs are active-low.

4.2.1 SINGLE-LED MODE

In single-LED mode, the **LED*x*_1** pin indicates the link status while the **LED*x*_0** pin indicates the activity status, as shown in Figure 4-2.

TABLE 4-2: SINGLE-LED MODE PIN DEFINITION

LED Pin	Pin State	Pin LED Definition	Link/Activity
LED*x*_1	H	OFF	Link Off
	L	ON	Link On (any speed)
LED*x*_0	H	OFF	No Activity
	Toggle	Blinking	Activity (RX,TX)

4.2.2 TRI-COLOR DUAL-LED MODE

In tri-color dual-LED mode, the link and activity status are indicated by the **LED*x*_1** pin for 1000BASE-T; by the **LED*x*_0** pin for 100BASE-TX; and by both **LED*x*_1** and **LED*x*_0** pins, working in conjunction, for 10BASE-T. This behavior is summarized in Figure 4-3.

TABLE 4-3: TRI-COLOR DUAL-LED MODE PIN DEFINITION

LED Pin (State)		LED Pin (Definition)		Link/Activity
LED*x*_1	**LED*x*_0**	**LED*x*_1**	**LED*x*_0**	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000Mbps Link / No Activity
Toggle	H	Blinking	OFF	1000Mbps Link / Activity (RX,TX)
H	L	OFF	ON	100Mbps Link / No Activity
H	Toggle	OFF	Blinking	100Mbps Link / Activity (RX,TX)
L	L	ON	ON	10Mbps Link / No Activity
Toggle	Toggle	Blinking	Blinking	10Mbps Link / Activity (RX,TX)

4.3 Media Access Controller (MAC)

4.3.1 MAC OPERATION

The device strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications, such as VoIP, where restricting certain packets reduces congestion and thus improves performance.

The transmit MAC takes data from the egress buffer and creates full Ethernet frames by adding the preamble and the start-of-frame delimiter ahead of the data, and generates the FCS that is appended to the end of the frame. It also sends flow control packets as needed.

The receive MAC accepts data via the integrated PHY or via the MII/RMII/RGMII interface. It decodes the data bytes, strips off the preamble and SFD of each frame. The destination and source addresses and VLAN tag are extracted for use in filtering and address/ID lookup, and the MAC also calculates the CRC of the received frame, which is compared to the FCS field. The MAC can discard frames that are the wrong size, that have an FCS error, or when the source MAC address matches the Switch MAC address.

The receive MAC also implements the Wake on LAN (WoL) feature. This system power saving feature is described in detail in the Section 4.10, "Power Management".

MIB statistics are collected in both receive and transmit directions.

4.3.2 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is specified as being between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is specified as being from carrier sense (CRS) to the next transmit packet.

4.3.3 BACK-OFF ALGORITHM

The device implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

4.3.4 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

4.3.5 LEGAL PACKET SIZE

On all ports, the device discards received packets smaller than 64 bytes (excluding VLAN tag, including FCS) or larger than the maximum size. The default maximum size is the IEEE standard of 1518 bytes, but can be programmed to 2000 bytes. Ports operating at 1000Mbps may be programmed to accept jumbo packets up to 9000 bytes, but for performance reasons it is recommended that no more than two ports be enabled simultaneously for jumbo packets.

4.3.6 FLOW CONTROL

The device supports standard MAC Control PAUSE (802.3x flow control) frames in both the transmit and receive directions for full-duplex connections.

In the receive direction, if a PAUSE control frame is received on any port, the device will not transmit the next normal frame on that port until the timer, specified in the PAUSE control frame, expires. If another PAUSE frame is received before the current timer expires, the timer will then update with the new value in the second PAUSE frame. During this period (while it is flow controlled), only flow control packets from the device are transmitted.

In the transmit direction, the device has intelligent and efficient ways to determine when to invoke flow control and send PAUSE frames. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The device issues a PAUSE frame containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the device sends out another flow control frame with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

4.3.7 HALF-DUPLEX BACK PRESSURE

A half-duplex back pressure option (non-IEEE 802.3 standard) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If back pressure is required, the device sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the device discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type back pressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T/Te or 100BASE-TX half-duplex modes, the user must enable the following:

- No excessive collision drop (Switch MAC Control 1 Register)
- Back pressure (Port MAC Control 1 Register)

4.3.8 FLOW CONTROL AND BACK PRESSURE REGISTERS

Table 4-4 provides a list of flow control and back pressure related registers.

TABLE 4-4: FLOW CONTROL AND BACK PRESSURE REGISTERS

Registers	Description
LED Configuration Strap Register	LED configuration strap settings. (**LED1_1** enables flow control and back pressure)
Switch MAC Address 0 Register through Switch MAC Address 5 Register	Switch's MAC address, used as source address of PAUSE control frames
Switch MAC Control 0 Register	“Aggressive back-off” enable
Switch MAC Control 1 Register	BP mode, “Fair mode” enable, “no excessive collision drop” enable
Switch MAC Control 4 Register	Pass PAUSE control frames
Port Status Register	Flow control enable (per port)
PHY Auto-Negotiation Advertisement Register	PHY - flow control advertisement (per port)
Port MAC Control 1 Register	Half-duplex back pressure enable (per port)
Port Ingress Rate Limit Control Register	Ingress rate limit flow control enable (per port)
Port Control 0 Register	Drop mode (per port)

4.3.9 BROADCAST STORM PROTECTION

The device has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The device has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BASE-TX and a 500ms interval for 10BASE-T/Te. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in control registers. The default setting equates to a rate of 1%.

4.3.10 SELF-ADDRESS FILTERING

Received packets can be filtered (dropped) if their source address matches the device's MAC address. This feature is useful for automatically terminating packets once they have traversed a ring network and returned to their source. It can be enabled on a per-port basis via the Switch Lookup Engine Control 1 Register and Port Control 2 Register.

4.4 Switch

4.4.1 SWITCHING ENGINE

A high-performance switching engine is used to move data to and from the MAC's packet buffers. It operates in store and forward mode, while an efficient switching mechanism reduces overall latency. The switching engine has a 256KByte internal frame buffer that is shared between all the ports.

For the majority of switch functions, all of the data ports are treated equally. However, a few functions such as IGMP snooping, 802.1X, forwarding invalid VLAN packets, etc., give special recognition to the host port. Any port (but most commonly port 6 or port 7) may be assigned as the host port by enabling tail tagging mode for that port. Only one port may be a host port.

When a switch receives a non-error packet, it checks the packet's destination MAC address. If the address is known, the packet is forwarded to the output port that is associated with the destination MAC address. The following paragraphs describe the key functions of destination address lookup and source address learning. These processes may be combined with VLAN support and other features, which are described in the subsequent sub-sections.

4.4.2 ADDRESS LOOKUP

Destination address lookup is performed in three separate internal address tables in the device:

1. Address Lookup (ALU) Table: 4K dynamic + static entries
2. Static Address Table: 16 static entries
3. Reserved Multicast Address Table: 8 pre-configured static entries

4.4.2.1 Address Lookup (ALU) Table

The Address Lookup (ALU) Table stores MAC addresses and their associated information. This table holds both dynamic and static entries. Dynamic entries are created automatically in hardware, as described in Section 4.4.2.4, "Learning". Static entries are created by management software.

This table is a 4-way associative memory, with 1K buckets, for a total of 4K entries. A hash function translates the received packet's MAC address (and optionally the FID) into a 10-bit index for accessing the table. At each bucket are four fully-associative address entries. All four entries are simultaneously compared to the MAC address (plus optional FID) for a possible match.

Three options are available for the hashing function, as described in Table 4-5. If VLAN is enabled (802.1Q VLAN Enable bit in the Switch Lookup Engine Control 0 Register), the VLAN group (FID) is included in the hashing function along with the MAC address. If VLAN is not enabled the hashing function is applied to MAC address and the FID in the default VLAN (VID=1) which is 0.

TABLE 4-5: ADDRESS LOOKUP TABLE HASHING OPTIONS

HASH_OPTION (Switch Lookup Engine Control 0 Register)	Description
01b (Default)	A hash algorithm based on the CRC of the MAC address plus FID. The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits [9:0] of the hash value plus (binary addition) 7-bit FID (zero extended on the left) are used as an index to the table. The CRC-CCITT polynomial is: $X^{16}+X^{12}+X^{5}+1$.
10b	An XOR algorithm based on 16 bits of the XOR of the triple-folded MAC address. Bits [9:0] of the XOR value plus 7-bit FID (left-extended) are used to index the table.
00b or 11b	A direct algorithm. The 10 least significant bits of the MAC address plus 7 bit FID are used to index the table.

4.4.2.2 Static Address Table

The 16-entry Static Address Table is typically used to hold multicast addresses, but is not limited to this. As with static entries in the ALU table, entries in the Static Address Table are created by management software. It serves the same function as static entries that are created in the ALU table, so its use is optional.

4.4.2.3 Reserved Multicast Address Table

The Reserved Multicast Address Table holds 8 pre-configured address entries, as defined in Table 4-6. This table is an optional feature that is disabled at power-on. If desired, the forwarding ports may be modified.

TABLE 4-6: RESERVED MULTICAST ADDRESS TABLE

Group	Address	MAC Group Address Function	Default PORT FORWARD Value (defines forwarding port: P7...P1)	Default Forwarding Action
0	(01-80-C2-00)-00-00	Bridge Group Data	100_0000	Forward only to the highest numbered port (default host port)
1	(01-80-C2-00)-00-01	MAC Control Frame (typically flow control)	000_0000	Drop MAC flow control
2	(01-80-C2-00)-00-03	802.1X Access Control	100_0000	Forward to highest numbered port
3	(01-80-C2-00)-00-10	Bridge Management	111_1111	Flood to all ports
4	(01-80-C2-00)-00-20	GMRP	011_1111	Flood to all ports except highest numbered port
5	(01-80-C2-00)-00-21	GVRP	011_1111	Flood to all ports except highest numbered port
6	(01-80-C2-00)-00-02, (01-80-C2-00)-00-04 – (01-80-C2-00)-00-0F		100_0000	Forward to highest numbered port
7	(01-80-C2-00)-00-11 - (01-80-C2-00)-00-1F, (01-80-C2-00)-00-22 - (01-80-C2-00)-00-2F		011_1111	Flood to all ports except highest numbered port

If a match is found in one of the tables, then the destination port is read from that table entry. If a match is found in more than one table, static entries will take priority over dynamic entries.

4.4.2.4 Learning

The internal lookup engine updates the ALU table with a new dynamic entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the lookup table.
- The received packet has no errors, and the packet size is of legal length.
- The received packet has a unicast SA.
- If VLAN is enabled, the received packet must belong to the indicated VLAN domain (FID).

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If all four table entries are valid, the oldest of the (up to four) dynamic entries may be deleted to make room for the new entry. Static entries are never deleted by the learning process. If all four entries are static entries, the address is not learned but an interrupt is generated and the table index number is made available to the interrupt service routine.

4.4.2.5 Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the ALU table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet has no receiving errors, and the packet size is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

4.4.2.6 Aging

The lookup engine updates the time stamp information of a dynamic record in the ALU table whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 300 seconds (±75 seconds) and can be configured longer or shorter (1 second to 30 minutes). This feature can be enabled or disabled. Static entries are exempt from the aging process.

4.4.2.7 Forwarding

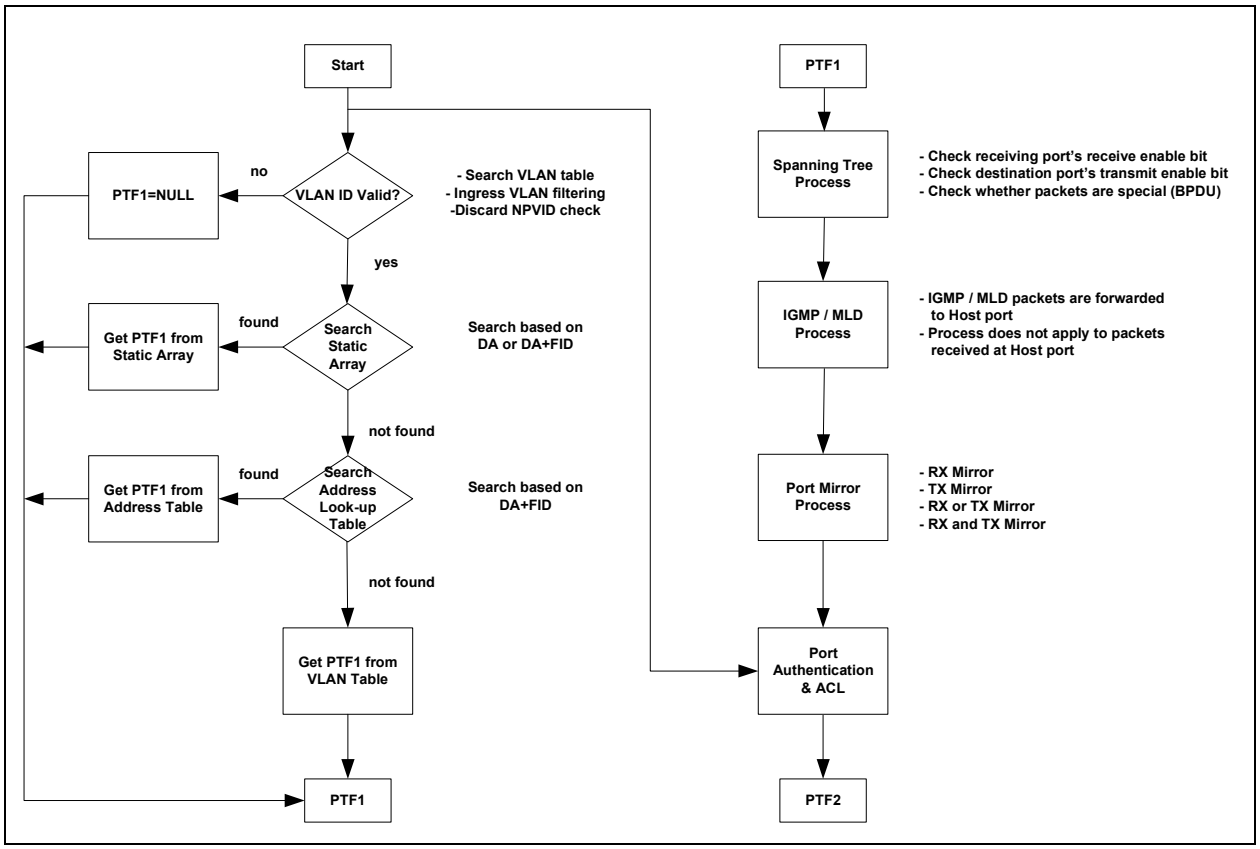
The device forwards packets using the algorithm that is depicted in Figure 4-3. Figure 4-3 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1" (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes.

The ACL process works in parallel with the flow outlined above. The authentication and ACL processes have the highest priority in the forwarding process, and the ACL result may override the result of the above flow. The output of the ACL process is the final “port-to-forward 2" (PTF2) destination port(s).

The device will not forward the following packets:

- Error packets: These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- MAC Control PAUSE frames: The device intercepts these packets and performs full duplex flow control accordingly.
- “Local” packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as “local”.
- In-Band Management packets.

FIGURE 4-3: PACKET FORWARDING PROCESS FLOWCHART



4.4.2.8 Lookup Engine Registers

Table 4-7 provides a list of lookup engine related registers.

TABLE 4-7: LOOKUP ENGINE REGISTERS

Registers	Description
Global Interrupt Status Register, Global Interrupt Mask Register	Top level LUE interrupt
Switch Lookup Engine Control 0 Register, Switch Lookup Engine Control 1 Register, Switch Lookup Engine Control 2 Register, Switch Lookup Engine Control 3 Register	Misc.
Address Lookup Table Interrupt Register, Address Lookup Table Mask Register	Low level LUE interrupts
Address Lookup Table Entry Index 0 Register, Address Lookup Table Entry Index 1 Register	Access failure address/index
ALU Table Index 0 Register, ALU Table Index 1 Register, ALU Table Access Control Register, Static Address and Reserved Multicast Table Control Register, ALU / Static Address Table Entry 1 Register, ALU / Static Address / Reserved Multicast Table Entry 2 Register, ALU / Static Address Table Entry 3 Register, ALU / Static Address Table Entry 4 Register	Address table access registers

4.4.3 IEEE 802.1Q VLAN

Virtual LAN is a means of segregating a physical network into multiple virtual networks whereby traffic may be confined to specific subsets of the greater network. IEEE 802.1Q defines a VLAN protocol using a 4-byte tag that is added to the Ethernet frame header. The device supports port-based and tag-based VLANs, including tagging, un-tagging, forwarding and filtering.

4.4.3.1 Non-Tag Port-Based VLAN

The simplest VLAN method establishes forwarding restrictions on a port-by-port basis without using VLAN tags. There is a register for each ingress port that is used to specify the allowed forwarding ports. An incoming packet is restricted from being forwarded to any egress port that is disallowed for that ingress port. The settings are made in the Port Control 1 Register. This function is always enabled; it is not enabled and disabled by the 802.1Q VLAN Enable bit in the Switch Lookup Engine Control 0 Register. The default setting is to allow all ingress-to-egress port paths.

4.4.3.2 Tag-Based VLAN

When 802.1Q VLAN is enabled, an internal VLAN Table with 4k entries is used to a store port membership list, VLAN group ID (FID) and additional information relating to each VLAN. This table must be set up by an administrator prior to enabling 802.1Q VLAN. Enabling is done by setting the 802.1Q VLAN Enable bit in the Switch Lookup Engine Control 0 Register.

In 802.1Q VLAN mode, the lookup process starts with VLAN Table lookup, using the tag's VID as the address. The first step is to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. Alternatively, unknown VID packets may be forwarded to pre-defined ports or to the host port. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (hashed(DA) + FID) are used to determine the destination port. The FID + Source Address (hashed(SA) + FID) are used for address learning (see Table 4-9 and Table 4-10).

The hashed(DA) + FID are hashed and used for forwarding lookup in the Address Lookup and Static Address Tables. For a successful address table lookup, the FID fields must also match. If the match fails, the packet is broadcast to all the VLAN port members defined in the VLAN Table entry. If there is a match and egress VLAN filtering is enabled, the packet is forwarded to those ports that are in both the address table port forwarding list and the VLAN table port membership list.

A similar address table lookup is performed using the hashed(SA) + FID. If the lookup fails, the FID and SA are learned.

If a non-tagged or null-VID-tagged packet is received, the ingress port default VID (Port Default Tag 0 Register and Port Default Tag 1 Register) is used for lookup.

Table 4-8 details the forwarding and discarding actions that are taken for the various VLAN scenarios. The first entry in the table is explained by the fact that VLAN Table lookup is enabled even when 802.1Q VLAN is not enabled. Notice that in the Port Default Tag 0 Register and Port Default Tag 1 Register, the port default VID is 1 for each port. Correspondingly, the VLAN port membership list in the VLAN Table entry for VID=1 is pre-configured at power-on to all ones. This provides the standard Ethernet switch behavior of broadcasting all packets with unknown destination address. If the VLAN table entry # 1 is changed, or if the port default VID is changed, this may affect the forwarding action for “unknown packets” even when VLAN is not enabled.

It should also be noted that the default values of the Egress VLAN Filtering bits are zero. These bits are zero only for backwards compatibility with previous “KSZ” switches. The resulting switch behavior, in the event of a successful VLAN and ALU lookups, is to forward the packet to the ports in the address table port forwarding list, without regard to the VLAN port membership list. It is suggested that the Egress VLAN Filtering bits be set to one so that the VLAN port membership list from the VLAN Table will be used to qualify the forwarding determined from the address lookup.

TABLE 4-8: VLAN FORWARDING

VLAN Enable (Note 4-1)	VLAN Match/ Valid (Note 4-2)	Forward Option (Note 4-3)	Egress VLAN Filtering (Note 4-4)	Unknown VID Forward (Note 4-5)	Drop Invalid VID (Note 4-6)	ALU Match/ Valid (Note 4-7)	Action
0	X	X	X	X	X	No	Forward to port membership list of default VID in LAN table
0	X	X	X	X	X	Yes	Forward to Address Lookup port forwarding list
1	No	X	X	0	0	X	Forward to host port
1	No	X	X	0 (def)	1 (def)	X	Discard
1	No	X	X	1	X	X	Forward to Unknown VID packet forward port list
1	Yes	0	X	X	X	No	**Broadcast:** Forward to VLAN table port membership list (PORT FORWARD) **Multicast:** Forward to Unknown Multicast ports if UM is enabled. Else, forward to VLAN table port membership list. **Unicast:** Forward to Unknown Unicast ports if UU is enabled. Else forward to VLAN table port membership list.
1	Yes	0	0 (def)	X	X	Yes	Forward to address table lookup port forwarding list
1	Yes	0	1	X	X	Yes	Forward to address table lookup port forwarding list & VLAN table port membership list (bitwise AND)
1	Yes	1	X	X	X	Yes	Forward to VLAN table port membership list

Note: "(def)" indicates the default power-up value.

Note 4-1 **VLAN Enable** is bit 7 in the Switch Lookup Engine Control 0 Register

Note 4-2 **VLAN Match/Valid** indicates when the VLAN Table entry is valid

Note 4-3 **Forward Option** is a bit in the VLAN Table Entry 0 Register

Note 4-4 **Egress VLAN Filtering** are bits 5 and 4 in the Switch Lookup Engine Control 2 Register

Note 4-5 **Unknown VID Forwarding** is in the Unknown VLAN ID Control Register

Note 4-6 **Drop Invalid VID** is bit 6 in the Switch Lookup Engine Control 0 Register

Note 4-7 **ALU Match/Valid** indicates when the Address Lookup is a success

Table 4-9 describes in more detail the address lookup process that follows the VLAN Table lookup. Lookup occurs in both the Address Lookup Table and the Static Address Table simultaneously, and the resulting action depends on the results of the two lookups.

TABLE 4-9: HASHED(DA) + FID LOOKUP IN VLAN MODE

DA found in Static MAC Table?	Use FID Flag? (Static MAC Table)	FID Match?	DA+FID found in ALU Table?	Action
No	Don't Care	Don't Care	No	Lookup has failed. Broadcast to the membership ports defined in the VLAN Table
No	Don't Care	Don't Care	Yes	Send to the destination port defined in the Address Lookup (ALU) Table
Yes	0	Don't Care	Don't Care	Send to the destination port(s) defined in the Static Address Table
Yes	1	No	No	Lookup has failed. Broadcast to the membership ports defined in the VLAN Table.
Yes	1	No	Yes	Send to the destination port defined in the Address Lookup (ALU) Table
Yes	1	Yes	Don't Care	Send to the destination port(s) defined in the Static Address Table

A source address (SA) lookup is also performed in the Address Lookup Table. SA lookup also performs SA filtering and MAC priority when the address is hit. Table 4-10 describes how learning is performed in the Address Lookup Table when a successful VLAN table lookup has been done and the no matching static entry is found in the Address Lookup Table or the Static Address Table.

TABLE 4-10: HASHED(SA) + FID LOOKUP IN VLAN MODE

FID + SA found in Address Lookup (ALU) Table?	Action
No	Learn and add FID + SA to the Address Lookup (ALU) Table
Yes	Update time stamp

4.4.3.2.1 Tag Insertion and Removal

Tag insertion is enabled on all ports when the VLAN feature is enabled. At the ingress port, untagged packets are tagged with the ingress port's default tag. The default tag is separately programmable for each port. The switch does not add tags to already tagged packets unless double tagging is enabled.

At the egress port, tagged packets will have their 802.1Q VLAN tags removed if un-tagging is enabled in the VLAN table entry. This feature is controlled on a per-port basis. Untagged packets will not be modified if 802.1Q is enabled.

4.4.3.2.2 Double Tagging

The switch supports double tagging, also known as Q-in-Q or VLAN stacking. This feature can be used for service providers to append a second VLAN tag in addition to a first VLAN tag applied by the customer. VLAN support can be enabled either with or without double tagging. When double tagging is enabled, the outer tag is recognized and is used for VLAN and address lookup instead of the inner tag. The outer tag precedes the inner tag in the frame header: the outer tag is located immediately after the source address, and contains a different Tag Protocol Identifier (TPID) value than the inner tag.

Additional controls are available for full control of the VLAN function. Some of these features can be enabled on a per-port basis, while others are global:

- **Ingress VLAN Filtering:** Discard packet if VID port membership in VLAN table does not include the ingress port.
- **Discard non PVID Packet:** Discard packet if VID does not match the ingress port default VID.
- **Discard un-tagged Packet:** Discard any received packet without a tag.
- **Drop tag:** Drops the packet if it is VLAN tagged.
- **Unknown VID Forward:** Forward to a fixed set of ports if VLAN lookup fails.
- **Drop unknown VID:** Additional options for unknown VID packets: discard or forward to the host port.
- **Null VID Replacement:** Replace a null VID with the ingress port default VID.
- **PVID Replacement:** Replace a non-null VID with the ingress port default VID.
- **Double Tag Mcast Trap:** In double tag mode, trap all reserved multicast packets and forward to the host port.

4.4.3.3 VLAN Registers

Table 4-11 provides a list of VLAN related registers.

TABLE 4-11: VLAN REGISTERS

Registers	Description
Switch Operation Register	Double tag enable
Switch Lookup Engine Control 0 Register	VLAN enable; Drop invalid VID frames
Switch Lookup Engine Control 2 Register	Trap double tagged MC frames; Dynamic & status egress VLAN filtering
Unknown VLAN ID Control Register	Forward unknown VID
Switch MAC Control 2 Register	Null VID replacement with PVID at egress
VLAN Table Entry 0 Register, VLAN Table Entry 1 Register, VLAN Table Entry 2 Register, VLAN Table Index Register, VLAN Table Access Control Register	Read/write access to the VLAN table
Port Default Tag 0 Register, Port Default Tag 1 Register	Port default tag
Port Ingress MAC Control Register	Drop non-VLAN frames; Tag drop
Port Transmit Queue PVID Register	PVID replacement at egress
Port Control 2 Register	VLAN table lookup for VID=0; Ingress VLAN filtering; PVID mismatch discard

4.4.4 QUALITY-OF-SERVICE (QOS) PRIORITY SUPPORT

The device provides quality-of-service (QoS) for applications such as VoIP. There are multiple methods for assigning priority to ingress packets. Depending on the packet prioritization method, the packet priority levels are mapped to the egress queues for each port. Each port can be configured for 1, 2, and 4 egress queues, which are prioritized. The default is 1 queue per port.

When configured for 4 priority queues, Queue 3 is the highest priority queue and Queue 0 is the lowest priority. Likewise, for a 2-queue configuration, Queue 1 is the highest priority queue. If a port is not configured as 2 or 4 queues, then high priority and low priority packets have equal priority in the single transmit queue.

There is an additional option for every port to select either to always deliver packets from the highest priority queue first, or use weighted round robin queuing amongst the multiple queues. This is described later in Section 4.4.13, "Scheduling and Rate Limiting".

4.4.4.1 Port-Based Priority

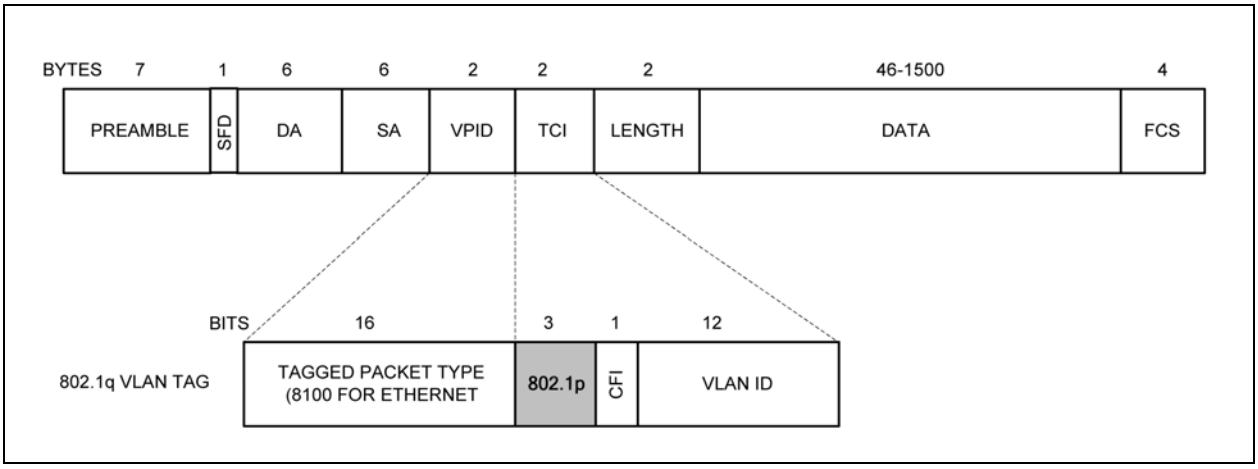
With port-based priority, each ingress port is individually classified as a specific priority level. All packets received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split into 2 or 4 queues.

4.4.4.2 IEEE 802.1p-Based Priority

For IEEE 802.1p-based priority, the device examines the ingress packets to determine whether they are tagged. If tagged, the 3-bit PCP priority field in the VLAN tag is retrieved and used to look up the “priority mapping” value. The “priority mapping” value is programmable.

Figure 4-4 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 4-4: 802.P PRIORITY FIELD FORMAT



4.4.4.3 IEEE 802.1p Priority Field Re-Mapping

This is a QoS feature that allows the device to set the “User Priority Ceiling” at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field.

4.4.4.4 DiffServ (DSCP) Priority (IP)

DiffServ-based priority from the DSCP field in the IP header can be used to determine packet priority. The 6-bit DSCP value is used as an index to a set of registers which translate the 6-bit DSCP value to a 2-bit value that specifies one of the 4 (or 2) queues. These registers are fully programmable.

4.4.4.5 ACL Priority

The Access Control List (ACL) Filtering feature can also be used to assign priority to received packets. This is discussed in Section 4.4.18, "Access Control List (ACL) Filtering".

4.4.5 TRAFFIC CONDITIONING & POLICING

4.4.5.1 Two Rate Three Color Marker

The Two Rate Three Color Marker meters an IP packet stream and marks its packets green, yellow, or red. A packet is marked red if it exceeds the Peak Information Rate (PIR). Otherwise, it is marked either yellow or green depending on whether it exceeds or doesn't exceed the Committed Information Rate (CIR).

The Meter operates in one of two modes. In the Color-Blind mode, the Meter assumes that the packet stream is uncolored. In the Color-Aware mode, the Meter assumes that some preceding entity has pre-colored the incoming packet stream so that each packet is green, yellow, or red. The Marker (re)colors an IP packet according to the results of the Meter.

4.4.5.2 Weighted Random Early Detection (WRED)

The WRED feature monitors the average queue size of packet memory and ingress queue size of each traffic class, and drops packets based on memory and queue utilization. If the buffers are almost empty, all incoming traffic is accepted. As the buffer utilization increases, the probability for dropping an incoming packet also increases.

WRED is intended to avoid the problem of global synchronization. Global synchronization can occur when a switch becomes congested and begins dropping incoming packets all at once. For TCP streams, packet drops invoke the TCP congestion control mechanism, which reduce the transmission rate until there are no more packet drops. If there are many TCP streams and their congestion control mechanisms act in unison, this can cause an undesirable oscillation in traffic rates. By selectively dropping some packets early rather than waiting until the buffer is full, WRED avoids dropping large numbers of packets at once and minimizes the chances of global synchronization.

The packet drop probability is based on the minimum threshold, maximum threshold, and a probability multiplier. When the average queue depth is above the minimum threshold, packets start getting dropped. The rate of packet drop increases linearly as the average queue size increases until the average queue size reaches the maximum threshold. The probability multiplier is the fraction of packets dropped when the average queue depth is at the maximum threshold. When the average queue size is above the maximum threshold, all packets are dropped.

AVB traffic streams (SR streams) can be exempted from WRED policing.

4.4.6 SPANNING TREE SUPPORT

To support spanning tree, one port is the designated port for the host processor, which is defined as the port for which tail tagging is enabled. Each of the other ports can be configured in one of the five spanning tree states via “transmit enable”, “receive enable” and “learning disable” register bits. Table 4-12 shows the setting and software actions taken for each of the five spanning tree states.

TABLE 4-12: SPANNING TREE STATES

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	transmit enable = 0 receive enable = 0 learning disable = 1	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the “Static MAC Table” with “overriding bit” set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded. Learning is disabled.	transmit enable = 0 receive enable = 0 learning disable = 1	The processor should not send any packets to the port(s) in this state. The processor should program the “Static MAC Table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**

TABLE 4-12: SPANNING TREE STATES (CONTINUED)

Only packets to and from the processor are forwarded. Learning is disabled.	transmit enable = 0 receive enable = 0 learning disable = 1	The processor should program the “Static MAC Table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	transmit enable = 0 receive enable = 0 learning disable = 0	The processor should program the “Static MAC Table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	transmit enable = 1 receive enable = 1 learning disable = 0	The processor programs the “Static MAC Table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

4.4.7 RAPID SPANNING TREE SUPPORT

There are three operational states assigned to each port for the Rapid Spanning Tree Protocol (RSTP):

1. Discarding State
2. Learning State
3. Forwarding State

4.4.7.1 Discarding State

Discarding ports do not participate in the active topology and do not learn MAC addresses.

- Discarding state: the state includes three states of the disable, blocking and listening of STP.
- Port setting: transmit enable = “0”, receive enable = “0”, learning disable = “1”.
- Software action: The host processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. When the port's learning capability (learning disable = '1') is disabled, port related entries in the ALU table and static MAC table can be rapidly flushed.

4.4.7.2 Learning State

Ports in “learning state” learn MAC addresses, but do not forward user traffic.

- Learning State: Only packets to and from the host processor are forwarded. Learning is enabled.
- Port setting for Learning State: transmit enable = “0”, receive enable = “0”, learning disable = “0”.
- Software action: The processor should program the Static Address Table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state (see Section 4.4.9, "Tail Tagging Mode" for details). Address learning is enabled on the port in this state.

4.4.7.3 Forwarding State

Ports in “forwarding states” fully participate in both data forwarding and MAC learning.

- Forwarding state: Packets are forwarded and received normally. Learning is enabled.
- Port setting: transmit enable = “1”, receive enable = “1”, learning disable = “0”.

- Software action: The host processor should program the Static Address Table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state (see Section 4.4.9, "Tail Tagging Mode" for details). Address learning is enabled on the port in this state.

RSTP uses only one type of BPDU called RSTP BPDUs. They are similar to STP configuration BPDUs with the exception of a type field set to “version 2" for RSTP and “version 0" for STP, and a flag field carrying additional information.

4.4.8 MULTIPLE SPANNING TREE SUPPORT

Multiple Spanning Tree Protocol (MSTP) is an extension of RSTP that allows different VLANs to have different spanning tree configurations. The VLAN Table, Address Lookup Table, Static Address Table and Reserved Multicast Address Table all contain a 3-bit field which can be used to specify one of eight spanning trees. Each port contains state registers for specifying unique states for each of the spanning trees.

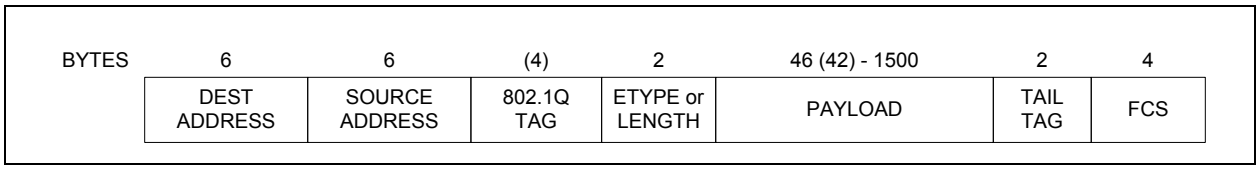
4.4.9 TAIL TAGGING MODE

Tail tagging is a method to communicate ingress and egress port information between the host processor and the switch. It is useful for spanning tree protocol, IGMP/MLD snooping, IEEE 1588, and other applications.

When the switch forwards a frame to the host port, two tail tagging bytes are added to the frame by the switch to indicate to the host processor the port that the frame was received on. In the other direction, the host processor adds the tail tagging bytes to a frame to indicate the intended egress destination port to the switch. When multiple priority queues are enabled, the tail tag is also used to indicate the priority queue. The tail tagging bytes are removed before the frame egresses the switch. Tail tagging may be enabled on any one port, and this defines the host port. tail tagging must not be enabled on multiple ports.

Tail tagging is implemented by inserting two additional bytes at the end of the packet, between the data field and the 4-byte CRC / FCS, as shown in Figure 4-5.

FIGURE 4-5: TAIL TAG FRAME FORMAT



4.4.10 IGMP SUPPORT

For Internet Group Management Protocol (IGMP) support in Layer 2, the device provides two components:

- “IGMP” Snooping
- “Multicast Address Insertion” in the Static MAC Table

4.4.10.1 “IGMP” Snooping

The device traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

Note:	The port for which Tail Tagging Mode is enabled is the host port.

4.4.10.2 “Multicast Address Insertion” in the Static MAC Table

Once the multicast address is programmed in the Static Address Table or Address Lookup Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

So that the host processor knows which port the IGMP packet was received on, Tail Tagging Mode must be enabled.

4.4.11 IPV6 MLD SNOOPING

The device traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to the processor (host port).

4.4.12 PORT MIRRORING

the device supports “port mirroring” comprehensively as:

- “Receive Only” Mirror-on-a-Port
- “Transmit Only” Mirror-on-a-Port
- “Receive and Transmit” Mirror-on-a-Port

4.4.12.1 “Receive Only” Mirror-on-a-Port

All the packets received on the port are mirrored on the sniffer port. For example, 1 is programmed to be “receive sniff” and the host port is programmed to be the “sniffer”. A packet received on port 1 is destined to port 2 after the internal lookup. The packet is forwarded to both port 2 and the host port. The device can optionally even forward “bad” received packets to the “sniffer port”.

4.4.12.2 “Transmit Only” Mirror-on-a-Port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and the host port is programmed to be the “sniffer port”. A packet received on port 2 is destined to port 1 after the internal lookup. The device forwards the packet to both port 1 and the host port.

4.4.12.3 “Receive and Transmit” Mirror-on-a-Port

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and the host port is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The device forwards the packet to both port 2 and the host port.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”.

4.4.13 SCHEDULING AND RATE LIMITING

Each device port has two egress packet scheduling options, which can be applied when the port is configured for two or four queues. Additionally, each port has ingress and egress rate limiter features.

4.4.13.1 Strict Priority Scheduling

When an egress port is configured as two or four queues, and strict priority scheduling is selected, each queue will take absolute priority over all lower priority queues. If a packet is available to transmit from queue 3 (the highest priority queue), then it will take priority for transmission over any packet that will also be available in any of the other queues. A packet in queue 2 will be transmitted only if no packet is available in queue 3. Weighted round robin is an alternative to strict priority scheduling.

4.4.13.2 Weighted Round Robin (WRR) Scheduling

WRR scheduling is an alternative to strict priority scheduling for egress queues. It is referred to as fair queuing because it gives proportionally higher priority to the highest priority queue, but not absolute priority.

4.4.13.3 Rate Limiting

The device supports independent ingress and egress hardware rate limiting on each port. Normally these two features are considered mutually exclusive, and users are discouraged from using both on the same port.

For 10BASE-T/Te, a rate setting above 10Mbps means the rate is not limited. Likewise, for 100BASE-TX, a rate setting above 100Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up ingress rate control registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up egress rate control registers. The size of each frame has options to include minimum inter-frame gap (IFG) or preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, the device provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The data rate from those selected type of frames is counted. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the leaky bucket algorithm is applied to each output priority queue for shaping output traffic. Inter-frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to ensure that the egress bandwidth exceeds the ingress bandwidth.

4.4.14 EGRESS TRAFFIC SHAPING

Two options are available for shaping the transmission of time-sensitive traffic: the IEEE 802.1Qav Credit-Based Traffic Shaper and the Time Aware Traffic Scheduler (TAS). The Credit-Based Shaper is defined in IEEE 802.1Qav for Audio Video Bridging (AVB). It attempts to minimize the jitter of traffic in the egress queue to which it applies, but the transmission of large packets from the “best effort” queue(s) can negatively impact its performance. The Time Aware Shaper reserves periodic time windows for the transmission of data from its queue. This ensures that low priority traffic will not block the periodic transmission of time-sensitive traffic, but it can also reduce the overall bandwidth of the port.

When a shaper is used, the corresponding egress ports are normally configured for either two or four queues. One or more queues may be used for time-sensitive (i.e. scheduled) traffic, and the remaining queue(s) are used for lower priority unscheduled (best effort) traffic. The shapers are applied on a per queue basis at each port. Shaping is individually configurable for each port and each queue.

The Credit-Based Shaper may be applied to either one or two queues on the same port. However, the Time Aware Scheduler may only be applied to one queue per port.

It is possible to use both the Time Aware Scheduler (TAS) and Credit based Shaper (CBS) options on the same port at the same time. The TAS and CBS queue/priority assignments are configured via software.

Section 4.4.4, "Quality-of-Service (QoS) Priority Support" discusses how ingress packets are mapped to egress queues based on priority. The most common method is by the PCP field of the VLAN tag.

4.4.14.1 IEEE 802.1Qav Credit-Based Traffic Shaper

The traffic shaper is used to meter high priority (AVB) egress traffic as determined by the reserved bandwidth of the SR class traffic. A separate traffic shaper is available at the egress of each priority queue at each port. If a port is configured for four queues, then the two highest priority queues may be used for SR traffic classes. If a port is configured for two queues, then the highest priority queue (1) may be used for the SR traffic class. The lower priority queue(s) are used for “best effort” class traffic and are configured for strict priority scheduling, with the traffic shaper disabled for these queues.

The traffic shaper is more sophisticated than the traditional “leaky bucket” rate limiting feature described earlier. A certain percentage of a port's bandwidth may be reserved for an AVB stream reservation (SR) traffic class. The traffic shaper may be configured for the reserved bandwidth, allowing the queue to egress packets at a rate up to but not exceeding this bandwidth. The queue may accumulate “credits” if an egress packet is delayed by a packet egressing from another queue. Accumulated credits may be used to permit catching up, in order to maintain an average rate.

If a traffic class supported by the credit-based shaper uses less than the bandwidth allocated to it, then the unused bandwidth can be used by other traffic classes, in accordance with the relative priorities of the traffic classes and the transmission queuing algorithms associated with them.

4.4.14.2 Time Aware Traffic Scheduler (TAS)

Like the Credit-Based Shaper, the Time Aware Scheduler is used to regulate the egress flow of high priority traffic. The TAS defines a periodic window of time during which only scheduled (high priority) traffic may egress a port. Additionally, transmission of low priority traffic will not be initiated during a guard band period prior to the high priority transmit window. This ensures that no blocking can occur during the transmit window.

The TAS is configured individually for each egress port. Typically the egress port shall be configured for multiple queues - either 2 or 4 - with at least one queue reserved for unscheduled “best effort” traffic. For each port, only one queue may be set up for TAS. With a 4-queue configuration, it is possible to have both TAS queue and one or two Credit-Based Shaper queues at the same time.

Once the guard band period begins, no packet transmission will be initiated unless the non-TAS queue packet length is smaller than the remaining guard band time. Any packets already being transmitted will be allowed to complete transmission. The guard band period shall be set up to match the transmit time for the largest possible non-scheduled packet. This ensures that transmission is always complete before the end of the guard band time. The guard band time is immediately followed by the transmit window. During the transmit window, transmission is allowed only for the TAS queue. All

other queues remain blocked. At the end of the transmit window, the block is lifted from all queues, and they are allowed to transmit per the scheduling scheme - either strict priority or weighted round robin (WRR). The cycle then repeats with start of the next guard band period.

A 128-entry table is used to define the time intervals that relate the guard band, transmit window and cycle time. The size of the table makes it possible to define two or more concurrent cycles which correspond to two or more individual streams. Each cycle can have a unique period, guard band and transmit window time.

4.4.15 LOW LATENCY CUT-THROUGH MODE

Cut-Through Mode allows for the reduction of packet latency through the switch by forwarding packets directly to the egress port without first waiting for receipt of the entire packet. This feature works in conjunction with the Time Aware Traffic Scheduler (TAS), and applies only if the incoming packet is being sent to a destination port with a corresponding TAS queue. Cut-through mode is enabled or disabled individually for each egress port.

Cut-through mode does not guarantee that all packets in the scheduled traffic class can be expedited. The following conditions must be met in order for cut-through to occur for a given packet. If the conditions are not met, the packet will be stored and queued in the usual manner.

- The Time Aware Scheduler must be applied to a queue at the egress port.
- The packet must belong to the scheduled traffic class that uses the Time Aware Scheduler.
- The TAS transmission window must be open.
- No other packet is currently being transmitted at that port.
- The TAS queue for that port is empty.
- The speed of the egress port must be equal to the speed of the ingress port.
- The packet must be unicast.

The only traffic going to a cut-through egress port should be a single unicast cut-through stream. The egress port may be configured as a single queue, with the Time Aware Scheduler applied to that one queue. Set the transmit window to 100%.

When cut-through occurs, the packet is forwarded after the first 64 bytes have been received. Latency through the switch is approximately 900ns for 1Gb/s traffic, regardless of the packet size. For non-cut-through packets, the minimum latency is proportional to the size of the packet.

4.4.16 INGRESS MAC ADDRESS FILTERING FUNCTION

When a packet is received, the destination MAC address is looked up in both the static and dynamic MAC address tables. If the address is not found in either of these tables, then the destination MAC address is “unknown”. By default, an unknown packet is forwarded to all ports except the port at which it was received. An optional feature makes it possible to specify the port or ports to which to forward unknown packets. It is also possible to specify no ports, meaning that unknown packets will be discarded. This feature is implemented separately for unknown unicast, unknown multicast and unknown VID packets.

4.4.17 802.1X ACCESS CONTROL

IEEE 802.1X is a Port-based authentication protocol. EAPOL is the protocol normally used by the authentication process as uncontrolled Port. By receiving and extracting special EAPOL frames, the host processor can control whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. The device detects EAPOL frames by checking the destination address of the frame. The destination addresses should be either a multicast address as defined in IEEE 802.1x (01-80-C2-00-00-03) or an address used in the programmable reserved multicast address domain with offset -00-03. Once EAPOL frames are detected, the frames are forwarded to the host port so it can send the frames to the authenticator server. Eventually, the CPU determines whether the requester is qualified or not based on its source MAC address, and frames are either accepted or dropped.

When the device is configured as an authenticator, the ports of the switch must then be configured for authorization. In an authenticator-initiated port authorization, a client is powered up or plugs into the port, and the authenticator port sends an Extensible Authentication Protocol (EAP) PDU to the supplicant requesting the identification of the supplicant. At this point in the process, the port on the switch is connected from a physical standpoint; however, the 802.1X process has not authorized the port and no frames are passed from the port on the supplicant into the switching fabric. If the supplicant attached to the switch (KSZ8567R) did not understand the EAP PDU that it was receiving from the switch, it

would not be able to send an ID and the port would remain unauthorized. In this state, the port would be blocked from passing any user traffic. If the supplicant is running the 802.1X EAP, it would respond to the request with its configured ID. (This could be a user name/password combination or a certificate.)

After the device receives the ID from the supplicant, it passes the ID information to an authentication server (RADIUS server) that can verify the identification information. The RADIUS server responds to the switch with either a success or failure message. If the response is a success, the port will be authorized and user traffic will be allowed to pass through the port like any switch port connected to an access device. If the response is a failure, the port will remain unauthorized and, therefore, unused. If there is no response from the server, the port will also remain unauthorized and will not pass any traffic.

Port control can be performed via the Access Control List (ACL) Filtering feature.

4.4.18 ACCESS CONTROL LIST (ACL) FILTERING

An Access Control List (ACL) can be created for each port to perform filtering on incoming layer 2 MAC, layer 3 IP or layer 4 TCP/UDP packets. Multicast filtering is handled in the Static Address Table and the Reserved Multicast Address Table, but the ACL provides additional capabilities for filtering routed network protocols. As shown in Figure 4-3, ACL filtering may take precedence over other forwarding functions.

The ACL allows the switch to filter ingress traffic based on the following header fields:

- Source or destination MAC address and/or EtherType
- Source or destination IPv4 address with programmable mask
- IPv4 protocol
- Source or destination UDP port
- Source or destination TCP port
- TCP Flag with programmable mask

The ACL is implemented as an ordered list of up to 16 access control rules which are programmed into the ACL Table. Each entry specifies certain rules (a set of matching conditions and action rules) to control the forwarding and priority of packets. When a packet is received on an interface, the switch compares the fields in the packet against any applied ACLs to verify that the packet has the permissions required to be forwarded, based on the conditions specified in the lists. Multiple match conditions can be either AND'ed or OR'ed together.

The ACL can also implement a count function that generates an interrupt rather than a forwarding action. The counter can be either a watchdog timer or an event counter. As a watchdog timer, an interrupt is generated if a packet with a specific MAC address and EtherType is not received within a specified time interval. As an event counter, an interrupt is generated once a specified number of packets with a specific MAC address and EtherType have been received.

The ACL consists of three parts: matching rules, action rules, and processing entries. A matching rule specifies what comparison test shall be performed on the incoming packet. It can also enable a counter function. An action rule specifies the forwarding action to be taken if the matching test succeeds. Alternatively, when a count function is enabled in a matching rule, the 11-bit count value is stored in the corresponding action rule field and there is no forwarding action.

In general, the 16 matching rules are not directly linked to the 16 action rules. For example, matching entry #0 is not necessarily related to action entry #0. The exception is when the counter function is enabled in a matching rule, whereby the matching rule and action rule fields at the same ACL table entry will function together and are no longer independent.

Each of the 16 processing entries is used to link any number of matching rules (specified in RuleSet) to any one action rule (specified in FRN). When there are multiple matching rules in a RuleSet, those rules are AND'ed together. Only if all of those matching results are true will the FRN action be taken.

It is also possible to configure the ACL table so that multiple processing entries specify the same action rule. In this way, the final matching result is the OR of the matching results from each of the multiple RuleSets.

The 16 ACL rules represent an ordered list, with entry #0 having the highest priority and entry #15 having the lowest priority. All matching rules are evaluated. If there are multiple true match results and multiple corresponding actions, the highest priority (lowest numbered) of those actions will be the one taken.

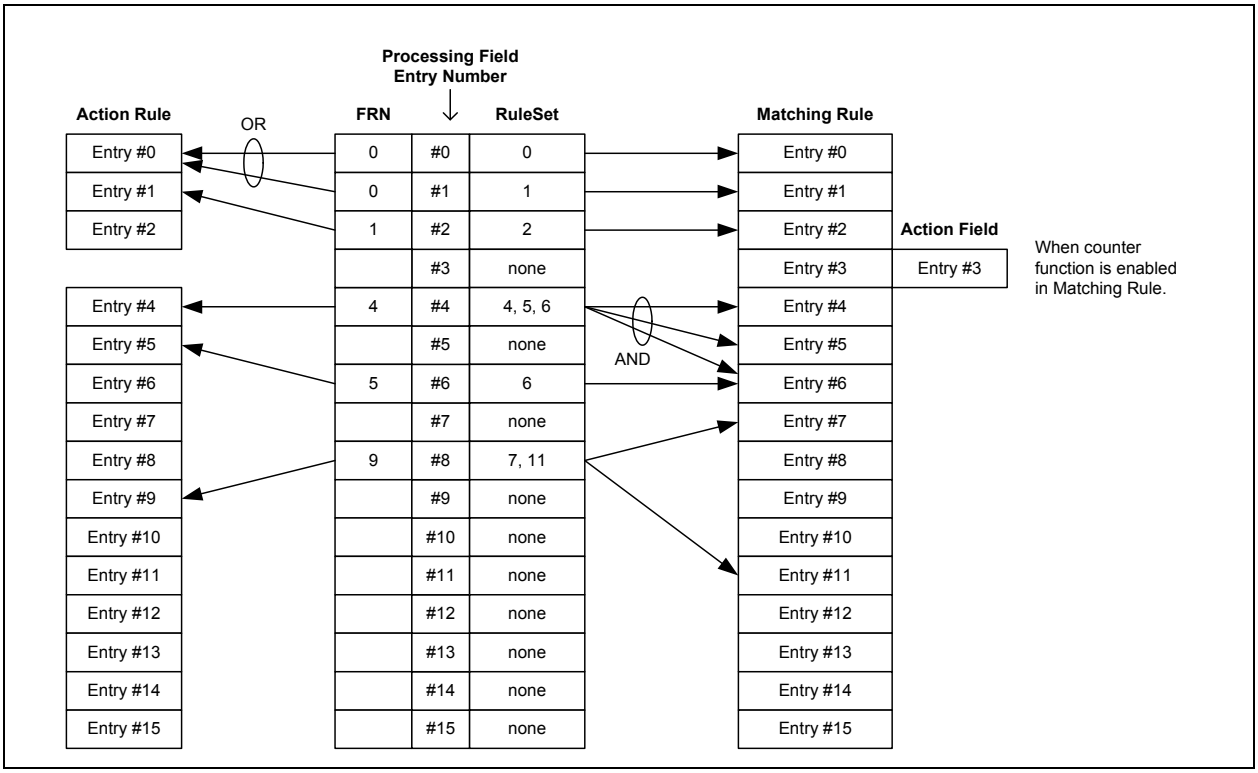
4.4.18.1 Processing Entry Description

The Processing Entry consists of two parameters as described in Table 4-13.

TABLE 4-13: ACL PROCESSING ENTRY PARAMETERS

Parameter	Description
FRN[3:0]	First Rule Number Pointer to an Action rule entry. Possible values are 0 to 15. If all Matching rules specified in the RuleSet are evaluated true, then this is the resulting Action rule.
RuleSet[15:0]	Specifies a set of one or more Matching rule entries. RuleSet has one bit for each of the 16 Matching rule entries. If multiple Matching rules are selected, then all conditions will be AND'ed to produce a final match result. 0 = Matching rule not selected 1 = Matching rule selected

FIGURE 4-6: ACL STRUCTURE AND EXAMPLE RULE VALUES



The examples in Figure 4-6 are interpreted as follows:

- Rule #0: Test the matching rule entry #0. If true, apply action rule entry #0.
- Rule #1: Test the matching rule entry #1. If true, apply action rule entry #0.
- Rule #2: Test the matching rule entry #2. If true, apply action rule entry #1.
- Matching rule entry #3 is configured for the counter function. Action entry #3 is used to hold the corresponding count value.
- Rule #4: Test the matching rule entries #4, 5 and 6. If all are true, apply action rule entry #4.
- Rule #6: Test the matching rule entry #6. If true, apply action rule entry #5.
- Rule #8: Test the matching rule entries #7 and 11. If both are true, apply action rule entry #9.

No more than one action can be taken for any packet. If the matching conditions are true for multiple RuleSets, then the corresponding FRN field with the lowest value (highest priority) determines the action to be taken.

Note that processing entries #0 and 1 produce an OR function: action #0 is taken if RuleSet #0 or RuleSet #1 is true.

Notice that processing entries #4 and 6 have overlapping RuleSets, but different FRNs. This can be summarized as:

If match #4, 5 and 6 are all true, then apply action #4,

Else if match #6 is true, then apply action #5.

Table 4-14 summarizes the available matching options. The MD and ENB fields are used to select the desired matching option. More configuration details are given in the following section.

TABLE 4-14: MATCHING RULE OPTIONS

MD[1:0]	ENB[1:0]	Matching Rule
00	XX	Matching rule disabled
01 (Layer 2 matching: MAC address, EtherType)	00	Action field is used as count value for packets matching MAC address and EtherType
	01	Compare MAC address only
	10	Compare EtherType only
	11	Compare both MAC address and EtherType
10 (Layer 3 matching: IP address)	00	Reserved
	01	Compare IPv4 source and destination address (with mask)
	10	Compare both source and destination IPv4 addresses (without mask)
	11	Reserved
11 (Layer 4 matching: TCP, UDP, IP protocol)	00	Compare IPv4 protocol
	01	Compare TCP source port or destination port
	10	Compare UDP source port or destination port
	11	Compare TCP sequence number

4.4.18.2 Matching Rule Description

The Matching Rule consists of several parameters. The first two parameters, MD[1:0] and ENB[1:0], determine the organization of the remainder of each Matching Rule.

When MD = 00, the Matching Rule is disabled.

TABLE 4-15: ACL MATCHING RULE PARAMETERS FOR MD = 01

Parameter	Description
MD[1:0]	MODE 00 = Matching rule is disabled 01 = Layer 2 MAC header or counter filtering 10 = Layer 3 IP header filtering 11 = Layer 4 TCP header (and IP protocol) filtering
ENB[1:0]	00 = Count Mode. Both the MAC Address and TYPE are tested. A count value (either time or packet count) is also incorporated. Details are given below this table. 01 = Comparison is performed only on the MAC Address value 10 = Comparison is performed only on the TYPE value 11 = Both the MAC Address and TYPE are tested
S/D	Source / Destination 0 = Destination address 1 = Source address
EQ	Equal / Not Equal 0 = Not Equal produces true result 1 = Equal produces true result
MAC ADDRESS[47:0]	48-bit MAC address
TYPE[15:0]	EtherType

Details for MD = 01, ENB = 00:

The 11 bits of the aggregated bit fields from PM, P, RPE, RP and MM in the Action rule entry specify a count value for packets matching MAC Address and TYPE in the Matching Field.

The count unit is determined by the TU bit (located in the Action rule).

- When 0, the unit is microsecond.
- When 1, the unit is millisecond.

The CA bit (located in the Action rule) determines the algorithm used to generate an interrupt when the count terminates.

- When 0, an 11-bit counter will be loaded with the count value from the list and start counting down every unit time. An interrupt will be generated when the timer expires, i.e. the next qualified packet has not been received within the period specified by the value.
- When 1, the counter is incremented with every matched packet received. An interrupt is generated when the terminal count is reached. The count resets thereafter. Time units are not used in this mode.

TABLE 4-16: ACL MATCHING RULE PARAMETERS FOR MD = 10

Parameter	Description
MD[1:0]	MODE 00 = Matching rule is disabled 01 = Layer 2 MAC header or counter filtering 10 = Layer 3 IP header filtering 11 = Layer 4 TCP header (and IP protocol) filtering
ENB[1:0]	00 = Reserved 01 = IPv4 source or destination address (with mask) 10 = IPv4 source and destination address (without mask) 11 = Reserved
S/D	Source / Destination 0 = Destination address 1 = Source address
EQ	Equal / Not Equal 0 = Not Equal produces true result 1 = Equal produces true result
IP ADDRESS[31:0]	IPv4 address Source or destination address (determined by S/D) when ENB = 01, Source address when ENB = 10
IP MASK[31:0]	Mask bits for the IPv4 address when ENB = 01: 0 = This bit of the address is compared 1 = This bit of the address is not compared Destination IPv4 address when ENB = 10

TABLE 4-17: ACL MATCHING RULE PARAMETERS FOR MD = 11

Parameter	Description
MD[1:0]	MODE 00 = Matching rule is disabled 01 = Layer 2 MAC header or counter filtering 10 = Layer 3 IP header filtering 11 = Layer 4 TCP header (and IP protocol) filtering
ENB[1:0]	00 = IP Protocol comparison is enabled 01 = TCP source/destination port comparison is enabled 10 = UDP source/destination port comparison is enabled 11 = TCP sequence number is compared
S/D	Source / Destination 0 = Destination address 1 = Source address

TABLE 4-17: ACL MATCHING RULE PARAMETERS FOR MD = 11 (CONTINUED)

Parameter	Description
EQ	Equal / Not Equal 0 = Not Equal produces true result 1 = Equal produces true result
MAX PORT[15:0] MIN PORT[15:0]	Max and Min Ports for TCP/UDP or TCP Sequence Number[31:0]
PC[1:0]	Port Comparison 00 = Port comparison is disabled 01 = Port matches either one of MAX or MIN 10 = Match if port number is in the range of MIN to MIN 11 = Match if port number is out of the range
PRO[7:0]	IPv4 protocol to be matched
FME	TCP Flag Match Enable 0 = TCP FLAG matching disabled 1 = TCP FLAG matching enabled
FMASK[7:0]	TCP FLAG Mask 0 = This bit of the Flag field is compared 1 = This bit of the Flag field is not compared
FLAG[7:0]	TCP Flag to be matched

4.4.18.3 Action Rule Description

TABLE 4-18: ACL ACTION RULE PARAMETERS FOR NON-COUNT MODES (MD ≠ 01 OR ENB ≠ 00)

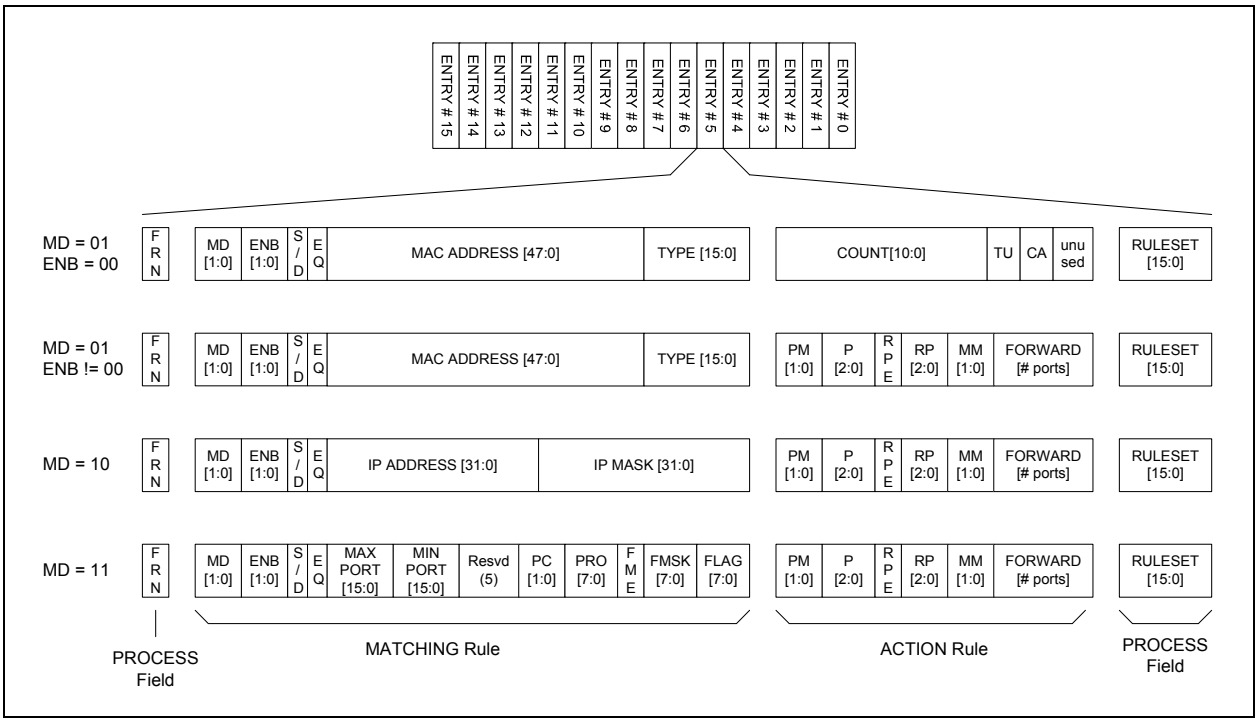
Parameter	Description
PM[1:0]	Priority Mode 00 = ACL does not specify the packet priority. Priority is determined by standard QoS functions. 01 = Change packet priority to P[2:0] if it is greater than QoS result. 10 = Change packet priority to P[2:0] if it is smaller than the QoS result. 11 = Always change packet priority to P[2:0].
P[2:0]	Priority value
RPE	Remark Priority Enable 0 = Disable priority remarking 1 = Enable priority remarking. VLAN tag priority (PCP) bits are replaced by RP[2:0].
RP[2:0]	Remarked Priority value
MM[1:0]	Map Mode 00 = No forwarding remapping 01 = The forwarding map in FORWARD is OR'ed with the forwarding map from the Address Lookup Table. 10 = The forwarding map in FORWARD is AND'ed with the forwarding map from the Address Lookup Table. 11 = The forwarding map in FORWARD replaces the forwarding map from the Address Lookup Table.
FORWARD[N-1:0]	Forwarding Ports Bit 0 corresponds to port 1 Bit 1 corresponds to port 2, etc. 0 = Do not forward to this port 1 = Forward to this port

TABLE 4-19: ACL ACTION RULE PARAMETERS FOR COUNT MODE (MD = 01 OR ENB = 00)

Parameter	Description
COUNT[10:0]	Count value
TU	Time unit for counter. 0 = Microseconds 1 = Milliseconds
CA	Counter Algorithm. 0 = An 11-bit counter will be loaded with the count value from the list and start counting down every unit time. An interrupt will be generated when the timer expires, i.e. the next qualified packet has not been received within the period specified by the value. 1 = The counter is incremented with every matched packet received. An interrupt is generated when the terminal count is reached. The count resets thereafter. Time units are not used in this mode.

Figure 4-7 shows basic organization of the ACL Table. The table has 16 entries, and each entry includes a matching field, action field and process field. Although these fields are stored together in one table, it is important to note that for a given table entry, the Matching, Action and Process fields generally do not form an associated group. The one exception is when the Matching Rule is in Count Mode (MD = 01 and ENB = 00). In that case, the Matching and Action fields are used in tandem.

FIGURE 4-7: ACL TABLE FORMAT



4.4.18.4 ACL Interrupts

The ACL filtering functions do not generate interrupts. Interrupts apply only for the Count Mode (MD = 01, ENB = 00). The Matching Rule can be configured either to timeout if the interval between packets of a specific type (MAC address and EtherType), or when a set number of these packets are received. There is a separate interrupt for each port. Port specific interrupt status and masks are located in the Port Interrupt Status Register and Port Interrupt Mask Register. The top level interrupt registers for each port are in the Global Port Interrupt Status Register and Global Port Interrupt Mask Register.

4.4.18.5 ACL Registers

Table 4-20 provides a list of ACL related registers.

TABLE 4-20: ACL REGISTERS

Registers	Description
Port Interrupt Status Register, Port Interrupt Mask Register	ACL interrupt
Port ACL Access 0 Register through Port ACL Access F Register, Port ACL Byte Enable MSB Register, Port ACL Byte Enable LSB Register, Port ACL Access Control 0 Register	ACL Table access
Port Priority Control Register	Priority classification
Port Authentication Control Register	ACL enable

4.5 IEEE 1588 Precision Time Protocol

The IEEE 1588 precision time protocol (PTP) provides a method for establishing time synchronization across nodes in a network. The device supports V2 (2008) of the IEEE 1588 PTP specification and can be programmed as either an end-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC) between ports. In addition, the host port can be programmed as either a slave or master ordinary clock (OC) port. Ingress timestamp capture, egress timestamp recording, correction field update with residence time and link delay, delay turn-around time insertion, egress timestamp insertion, and checksum update are supported. PTP frame filtering is implemented to enhance overall system performance. Delay adjustments are implemented to fine tune the synchronization. Versatile event trigger outputs and timestamp capture inputs are implemented to meet various real time application requirements through the **GPIO_1** pin.

The key features of the IEEE 1588 implementation are:

- Either one-step or two-step event message format
- Implementation of precision time clock per specification
  - Upper 16 bits of the second clock not implemented
- Both E2E and P2P TC
- Both slave and master OC
- PTP multicast and unicast addressing
- Transport of PTP over IPv4/IPv6 UDP and IEEE 802.3/Ethernet
- Precision time stamping of input signal on the **GPIO_1** pin
- Creation and delivery of clock, pulses, or other unique serial bit stream on the **GPIO_1** pin with respect to the precision time clock time.
- IEEE 802.1AS gPTP supported

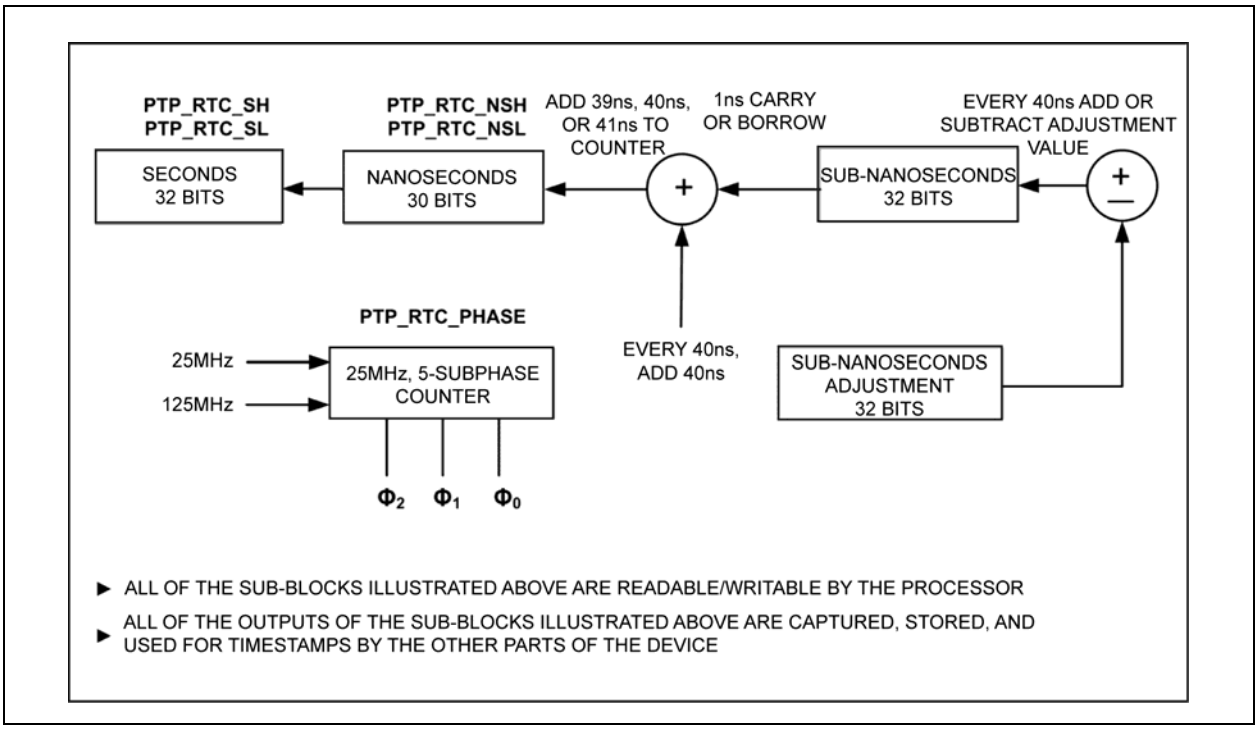
IEEE 1588 defines two essential functions: The measurement of link and residence (switching) delays by using the Delay_Req/Resp or Pdelay_Req/Resp messages, and the distribution of time information by using the Sync/Follow_Up messages. The 1588 PTP event messages are periodically sent from the grandmaster in the network to all slave clock devices. Link delays are measured by each slave node to all its link partners to compensate for the delay of PTP messages sent through the network.

4.5.1 IEEE 1588 PTP SYSTEM TIME CLOCK

The device's system time clock (STC) is a readable and writable high-precision counter that is used to keep the PTP time. The counter resolution is 2^{-32}ns. Figure 4-8 details the PTP Clock.

.

FIGURE 4-8: PTP SYSTEM CLOCK OVERVIEW



4.5.2 IEEE 1588 PTP MESSAGING PROCESSING

The device supports IEEE 1588 PTP time synchronization when 1588 PTP mode and message detection are enabled. Different operations will be applied to PTP packet processing based on the setting of P2P or E2E in transparent clock mode, master or slave in ordinary clock mode, one-step or two-step clock mode, and if the domain checking is enabled. For the IPv4/UDP egress packet, the checksum can be updated by either re-calculating the two-bytes or by setting it to zero. For the IPv6/UDP egress packet, the checksum is always updated.

4.5.3 IEEE 1588 PTP EVENT TRIGGERING AND TIMESTAMPING

An event trigger output signal can be generated when the target and activation time matches the IEEE1588 PTP system clock time. Likewise, an event timestamp input can be captured from an external event input signal and the corresponding time on the IEEE1588 PTP system clock will be captured. Both the output event block and the input timestamp block can be programmed to generate interrupts.

4.6 Audio Video Bridging and Time Sensitive Networks

AVB defines a set of features and protocols for ensuring high QoS for time-sensitive traffic such as audio and video streams. The device provides the necessary hardware features for implementation of AVB: gPTP timing synchronization features (802.1AS, based on 1588 PTP), prioritized queuing, and credit-based traffic shapers (802.1Qav). Ports supporting AVB must operate at 100 Mbps at full-duplex. 10 Mbps and/or half-duplex are not compatible with AVB.

Non-AVB devices are not allowed to participate in an AVB network, but non-AVB traffic is allowed to occupy available bandwidth unused by the AVB traffic. Protocols are defined for network discovery, path setup, and bandwidth reservation across the network.

AVB defines Stream Reservation (SR) traffic classes, which are given a high priority for queuing and egress scheduling. With up to four egress queues per port, the device can accommodate up to two SR traffic classes. Ingress AVB traffic packets are typically VLAN tagged. If not, the device can assign them a customizable VLAN tag on a port-by-port basis. The information in this tag, including the 3-bit PCP priority field, is used to map the packets to the appropriate high priority queue. At least one queue must be reserved for non-SR traffic classes, in order to accommodate regular “best effort” network traffic.

The egress of SR class traffic from the high priority queue(s) is regulated at each queue by a credit-based traffic shaper as discussed below. If the SR traffic streams do not exceed their reserved bandwidth, then the traffic shaper will ensure that the packets egress in a relatively uniform manner.

The 802.1AS standard, which ensures node synchronization in an AVB network, relies heavily on the IEEE 1588 standard for PTP. It defines a specific profile for 1588, and adds certain other requirements in the context of 802.1Q. The resulting entity is referred to as generalized PTP (gPTP). Section 4.5, "IEEE 1588 Precision Time Protocol" discusses IEEE 1588 and 802.1AS together.

The device provides two egress traffic shaping options. The IEEE 802.1Qav Credit-Based Traffic Shaper provides traffic shaping as defined in IEEE 802.1Qav. This is configurable on a per-queue basis. Each port also has a Time Aware Traffic Scheduler (TAS) that provides periodic timing windows for transmission of time sensitive traffic class data. The shaper and scheduler options and details are individually configurable for each egress port.

4.7 NAND Tree Support

The KSZ8567R provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8567R digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the **INTRP_N** pin provides the output for the last NAND gate.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving low each NAND tree input pin sequentially per the NAND tree pin order, starting with the first row of Table 4-21.
- Checking the NAND tree output to ensure there is a toggle high-to-low or low-to-high for each NAND tree input driven low.

TABLE 4-21: NAND TREE TEST PIN ORDER

NAND Tree Sequence	Pin Number	Pin Name	NAND Tree Description
1	48	**TX_CLK6/REFCLKI6**	Input
2	49	**TX_EN6/TX_CTL6**	Input
3	50	**TX_ER6**	Input
4	51	**COL6**	Input
5	52	**TXD6_3**	Input
6	53	**TXD6_2**	Input
7	54	**TXD6_1**	Input
8	55	**TXD6_0**	Input
9	57	**RX_CLK6/REFCLKO6**	Input
10	58	**RX_DV6/CRS_DV6/RX_CTL6**	Input
11	59	**RX_ER6**	Input
12	60	**CRS6**	Input
13	62	**RXD6_3**	Input
14	63	**RXD6_2**	Input
15	64	**RXD6_1**	Input
16	65	**RXD6_0**	Input
17	66	**TX_CLK7/REFCLKI7**	Input
18	67	**TX_EN7/TX_CTL7**	Input
19	68	**TX_ER7**	Input
20	69	**COL7**	Input
21	70	**TXD7_3**	Input
22	71	**TXD7_2**	Input
23	72	**TXD7_1**	Input

TABLE 4-21: NAND TREE TEST PIN ORDER (CONTINUED)

NAND Tree Sequence	Pin Number	Pin Name	NAND Tree Description
24	73	**TXD7_0**	Input
25	75	**RX_CLK7/REFCLKO7**	Input
26	76	**RX_DV7/CRS_DV7/RX_CTL7**	Input
27	78	**RX_ER7**	Input
28	79	**CRS7**	Input
29	80	**RXD7_3**	Input
30	81	**RXD7_2**	Input
31	82	**RXD7_1**	Input
32	83	**RXD7_0**	Input
33	85	**LED4_0**	Input
34	86	**LED4_1**	Input
35	88	**LED3_0**	Input
36	89	**LED3_1**	Input
37	90	**GPIO_1**	Input
38	91	**LED2_0**	Input
39	92	**LED2_1**	Input
40	93	**PME_N**	Input
41	96	**RESET_N**	Input
42	97	**SDO**	Input
43	98	**SDI/SDA/MDIO**	Input
44	100	**SCS_N**	Input
45	101	**SCL/MDC**	Input
46	102	**LED5_0**	Input
47	103	**LED5_1**	Input
48	105	**LED1_0**	Input
49	106	**LED1_1**	Input
50	94	**INTRP_N**	Output

The following procedure can be used to check for faults on the KSZ8567R digital I/O pin connections to the board:

1. Enable NAND tree mode via the **LED2_1**, **LED2_0**, and **LED4_0** configuration strap pins option.
2. Use board logic to drive all KSZ8567R NAND tree input pins high and verify that the **INTRP_N** pin output is high.
3. Use board logic to drive each NAND tree input pin, per the NAND Tree pin order, as follows:
   a) Toggle the first pin in the NAND tree sequence (**TX_CLK6/REFCLKI6**) from high to low, and verify the **INTRP_N** pin switches from high to low to indicate that the first pin is connected properly.
   b) Leave the first pin (**TX_CLK6/REFCLKI6**) low.
   c) Toggle the second pin in the NAND tree sequence (**TX_EN6/TX_CTL6**) from high to low, and verify the **INTRP_N** pin switches from low to high to indicate that the second pin is connected properly.
   d) Leave the first pin (**TX_CLK6/REFCLKI6**) and the second pin (**TX_EN6/TX_CTL6**) low.
   e) Toggle the third pin in the NAND tree sequence (**TX_ER6**) from high to low, and verify the **INTRP_N** pin switches from high to low to indicate that the third pin is connected properly.
   f) Continue with this sequence until all KSZ8567R NAND tree input pins have been toggled.

Each KSZ8567R NAND tree input pin must cause the **INTRP_N** output pin to toggle high-to-low or low-to-high to indicate a good connection. If the **INTRP_N** pin fails to toggle when the KSZ8567R input pin toggles from high to low, the input pin has a fault.

4.8 Clocking

4.8.1 PRIMARY CLOCK

The device requires a 25MHz reference clock input at the **XI** pin. This clock is internally multiplied up and used to clock all of the internal logic and switching functions. It is also normally used as to clock the PHY transmit paths. This clock may be supplied by connecting a crystal between the **XI** and **XO** pins (and appropriate load capacitors to ground). Alternatively, an external CMOS clock signal may drive **XI**, while **XO** is left unconnected. The **XI/XO** block is powered from **AVDDH**.

4.8.2 MAC INTERFACE CLOCKS

The MII interface is clocked asymmetrically, with the PHY device driving both the **RX_CLK*x*** receive clock and the **TX_CLK*x*** transmit clock to the MAC device. Each MII port may be configured at reset by a strapping option to take the role of either the PHY or the MAC. **RX_CLK*x*** and **TX_CLK*x*** are therefore either both inputs or both outputs, depending on the MII mode.

The RMII interface uses a single 50MHz clock. This REFCLK may be sourced either from the KSZ8567R or from the connected device. A strapping option is used to select the mode for each port. “Normal Mode” is the mode where the other device supplies the clock, and the clock is an input to the **REFCLKI*x*** pin of the device. “Clock Mode” is the mode where the KSZ8567R generates the 50MHz clock on the **REFCLKO*x*** pin.

The RGMII interface employs source synchronous clocking, so it is symmetrical and does not require a mode selection. An output clock is generated on the **RX_CLK*x*** pin, while an input clock is received on the **TX_CLK*x*** pin. The clock speed scales with the interface data rate - either 10, 100 or 1000 Mbps. A strapping option is used to select between the 100 and 1000 Mbps speeds. If the 10 Mbps rate is required, then a register setting is used to set that speed.

The MAC interfaces are powered from **VDDIO**.

Note:	Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information on using configuration straps.

4.8.3 SERIAL MANAGEMENT INTERFACE CLOCK

Whether configured to be SPI, I^2C or MIIM, the KSZ8567R is always a slave and receives the clock as an input. The serial management interface is powered from **VDDIO**.

4.8.4 SYNCHRONOUS ETHERNET AND SYNCLKO

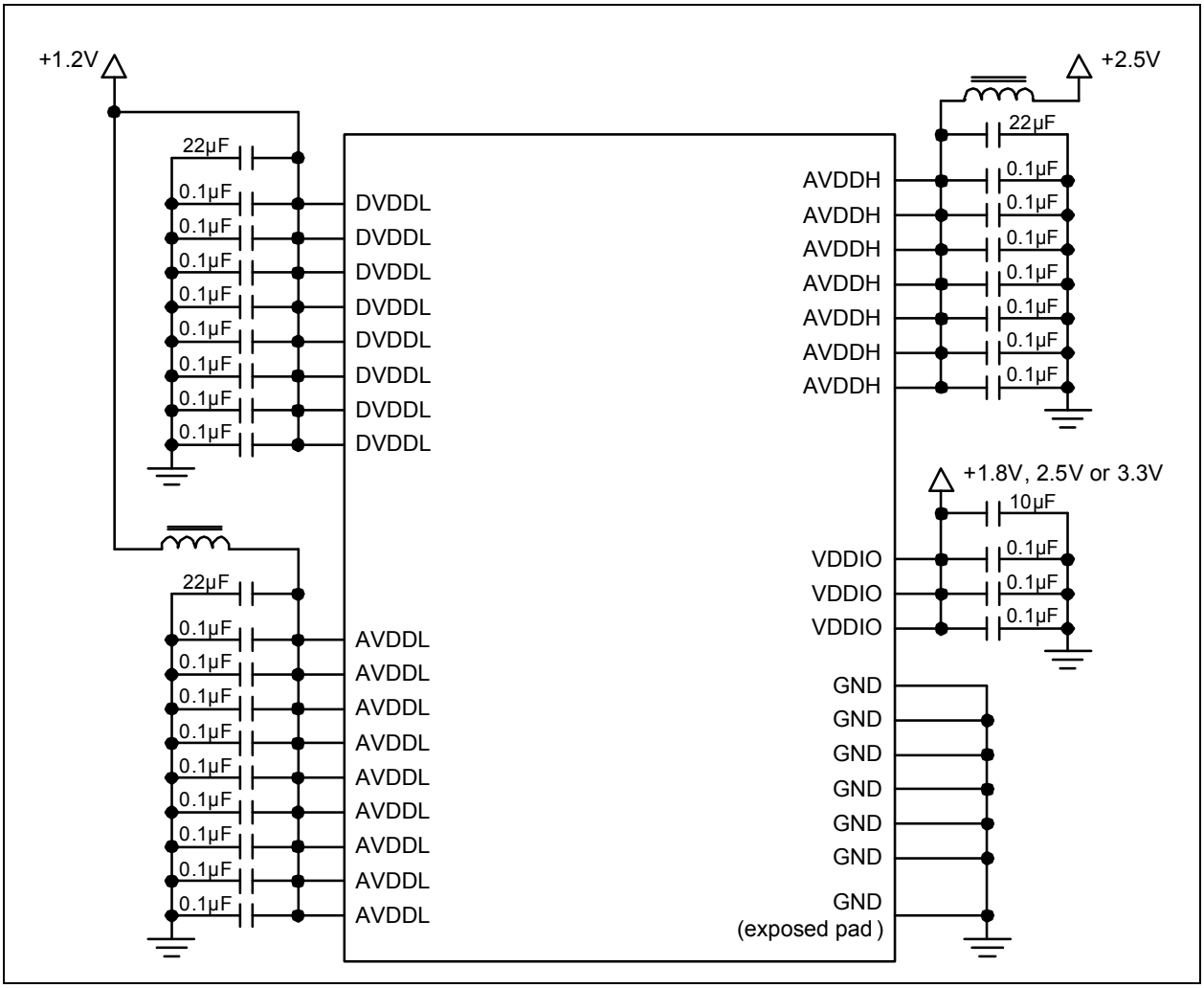
An output clock is provided on the **SYNCLKO** pin. By default it is derived from the 25MHz input reference clock on **XI**, but the source can be selected to be the recovered clock from any of the PHY ports. This recovered clock may then feed an external device with a low bandwidth PLL and hold-over feature for use in Synchronous Ethernet applications. A 25MHz clock derived from **SYNCLKO** may then be used as the input to **XI**.

The output frequency choices are 25MHz (default) and 125MHz. If not needed, this output clock can also be disabled. **SYNCLKO** is controlled via the Output Clock Control Register, and is powered from **VDDIO**.

4.9 Power

The KSZ8567R requires two to three supply voltages. The device core operates from a 1.2V supply (**DVDDL** and **AVDDL**). The PHY transceivers and XI/XO crystal/clock interface operate from a 2.5V or 3.3V supply (**AVDDH**). The digital I/O's can be operated from 1.8V, 2.5V or 3.3V (**VDDIO**). The digital I/Os powered from **VDDIO** include RGMII, RMII, MII, SPI, I^2C, MIIM, LED, **RESET_N**, **PME_N**, **INTRP_N** and **SYNCLKO**. An example power connection diagram can be seen in Figure 4-9.

FIGURE 4-9: POWER CONNECTION DIAGRAM



4.10 Power Management

The device supports enhanced power management features in a low-power state with energy detection to ensure low-power dissipation during device idle periods. There are three operation modes under the power management function which are implemented globally (i.e., applying to all ports):

- Normal Operation Mode
- Energy Detect Mode
- Global Soft Power Down Mode

Table 4-22 summarizes all internal function blocks status under the three power-management operation modes.

TABLE 4-22: MDI/MDI-X PIN DEFINITIONS

Functional Blocks	Power Management Operation Modes		
	Normal Mode	Energy Detect Mode	Soft Power Down Mode
Internal PLL Clock	Enabled	Disabled	Disabled
TX/RX PHYs	Enabled	Energy Detect at RX	Disabled
MACs	Enabled	Disabled	Disabled
Host Interface	Enabled	Disabled	Disabled

There are two additional power saving modes that may be implemented on a per-port basis:

- Port-Based Power Down
- Energy Efficient Ethernet (EEE) - Active only if enabled in the device and auto-negotiated (per-port) with a link partner. EEE can be enabled on a per-port basis, but is not available on the non-PHY ports 6 and 7.

The first three global power modes are mutually exclusive; only one mode may be selected at a time. Port-based power down may be enabled independent of the global power mode.

4.10.1 NORMAL OPERATION MODE

At power-up, the device enters into Normal operation mode. It is also selected via bits [4:3] = 00 in the Power Down Control 0 Register. When the device is in normal operation mode, all PLL clocks are running, PHYs and MACs are on, and the CPU is ready to read or write the device registers through the serial interface (SPI, I^2C or MIIM).

During normal operation mode, the host processor can change the power management mode bits in the Power Down Control 0 Register to transition to any of the other power management modes.

4.10.2 ENERGY-DETECT MODE

Energy-detect mode, also known as energy-detect power down (EDPD) mode, is enabled by setting bits [4:3] to 01 in the Power Down Control 0 Register. Energy-detect mode provides a mechanism to save power when the device is not connected to an active link partner. Auto-negotiation must be enabled when in energy-detect mode.

Energy-detect mode consists of two states, normal-power state and low-power state. When the device is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than a pre-configured value, the device will go into the low-power state. While in low-power state, the device reduces power consumption by disabling all circuitry except the energy-detect circuitry of the receiver, which consumes minimal power. When the device is in the low-power state, it will transmit link pulses at long intervals, with a very low duty cycle. At the same time, it continuously monitors for energy on the cable. Once energy is detected from the cable and is present for a time longer than 100ns, the device will enter the normal-power state.

4.10.3 GLOBAL SOFT POWER-DOWN MODE

Soft power-down mode is used to power down the device when it is not in use after power-up. This mode disables all internal functions except for the serial (SPI or I^2C) management interface.

When soft power-down mode is exited, all registers are reset to their default values, and all configuration strap pins are sampled to set the device settings.

4.10.4 PORT-BASED POWER DOWN

Unused ports may be powered down individually to save power.

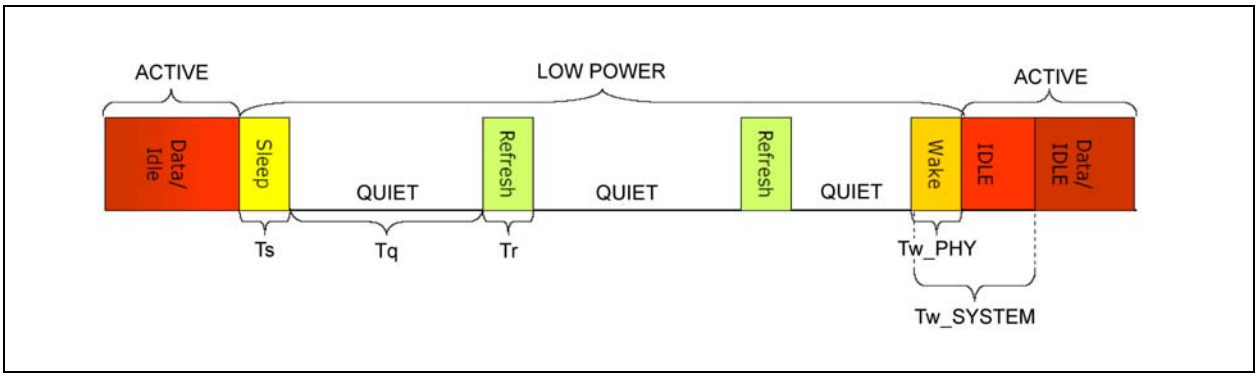
4.10.5 ENERGY EFFICIENT ETHERNET (EEE)

Energy-efficient Ethernet (EEE) is implemented in the device as described in the IEEE 802.3AZ specification for ports 1 through 5. EEE is not available on ports 6 and 7. EEE saves power by keeping the voltage on the Ethernet cable at approximately 0V for as often as possible during periods of no traffic activity. This is called the low-power idle (LPI) state. However, the link will respond automatically when traffic resumes and do so in such a way as to not cause blocking or dropping of any packets (the wake-up time for 100BASE-TX is specified to be less than 30µs). The transmit and receive directions are independently controlled.

The EEE feature is disabled by default. EEE must be auto-negotiated, and is enabled only if both nodes on a link support it.

The time during which LPI mode is active is called quiet time. This is shown in Figure 4-10.

FIGURE 4-10: TRAFFIC ACTIVITY AND EEE



4.10.5.1 Transmit Direction Control for MII Mode

For EEE ports, low-power idle (LPI) state for the transmit direction will be entered when the internal EEE MAC signals to its PHY to do so. The PHY will stay in the transmit LPI state as long as indicated by the MAC. The **TX_CLK*x*** is not stopped.

Even though the PHY is in LPI state, it will periodically leave the LPI state to transmit a refresh signal using specific transmit code bits. This allows the link partner to keep track of the long-term variation of channel characteristics and clock drift between the two partners. Approximately every 20ms - 22ms, the PHY will transmit a bit pattern to its link partner of duration 200µs - 220µs. The refresh times are shown in Figure 4-10.

4.10.5.2 Receive Direction Control for MII Mode

If enabled for LPI mode, upon receiving a P Code bit pattern (refresh), the PHY will enter the LPI state and signal to the internal MAC. If the PHY receives some non-P Code bit pattern, it will signal to the MAC to return to “normal frame” mode. The PHY can turn off the **RX_CLK*x*** after nine or more clocks have occurred in the LPI state.

In the EEE-compliant environment, the internal PHYs will be monitoring and expecting the P Code (refresh) bit pattern from its link partner that is generated approximately every 20ms - 22ms, with a duration of about 200µs - 220µs. This allows the link partner to keep track of the long term variation of channel characteristics and clock drift between the two partners.

4.10.6 WAKE ON LAN (WOL)

Wake on LAN allows a computer to be turned on or woken up by a network message. The message is usually sent by a program executed on another computer on the same local area network. Wake-up frame events are used to awaken the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. The device can be programmed to notify the host of the Wake-Up frame detection with the assertion of the power management event signal (**PME_N**).

The device’s MACs support the detection of the following Wake-Up events:

- Detection of energy signal over a pre-configured value
- Detection of a linkup in the network link state
- Receipt of a Magic Packet

There are also other types of Wake-Up events that are not listed here as manufacturers may choose to implement these in their own way.

4.10.6.1 Direction of Energy

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

4.10.6.2 Direction of Link-up

Link status wake events are useful to indicate a linkup in the network's connectivity status.

4.10.6.3 Magic Packet™

The Magic Packet is a broadcast frame containing anywhere within its payload 6 bytes of all 1s (FF FF FF FF FF FF) followed by sixteen repetitions of the target computer's 48-bit DA MAC address. Since the magic packet is only scanned for the above string, and not actually parsed by a full protocol stack, it may be sent as any network- and transport-layer protocol.

Magic Packet technology is used to remotely wake up a sleeping or powered-off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up. Once the device has been enabled for Magic Packet Detection, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE MAC address, or a multicast or broadcast address and CRC. The specific sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

4.10.6.4 Interrupt Generation on Power Management Related Events

There are two ways an interrupt can be generated to the host whenever a power management related event takes place. The resulting interrupts are via the **PME_N** signal pin or via the **INTRP_N** signal pin.

4.11 Management Interface

The management interface may be used by an external host processor to read and write the device's registers. This interface has three available modes of operation: SPI, I^2C or MIIM. The interface mode is selected at the deassertion of reset by a strapping option (refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information).

Of the three interface options, SPI provides the highest performance, while MIIM performance is the lowest. Most importantly, MIIM provides access to the PHY control and status registers, but not to any of the switch registers. The vast majority of applications therefore can use SPI or I^2C, but not MIIM.

Register access is also available through the high-performance in-band management interface as described in Section 4.12, "In-Band Management," on page 58.

4.11.1 SPI SLAVE BUS

The KSZ8567R supports a slave mode SPI interface that provides complete access to all device registers via an SPI master device. The SPI master device supplies the clock (**SCL**), select (**SCS_N**), and serial input data (**SDI**). Serial output data (**SDO**) is driven by the KSZ8567R.

SCL is expected to stay low when SPI operation is idle. SPI operations start with the falling edge of **SCS_N** and end with the rising edge of **SCS_N**. A single read or write access consists of a 27-bit command/address phase, then a 5-bit turnaround (TA) phase, then an 8-bit data phase. For burst read or write access, **SCS_N** is held low while **SCL** continues to toggle. For every 8 cycles of **SCL**, the device will increment the address counter, and the corresponding data byte will be transferred on **SDI** or **SDO** in succession.

All commands, addresses and data are transferred most significant bit first. Input data on **SDI** is latched on the rising edge of clock **SCL**. Output data on **SDO** is clocked on the falling edge of **SCL**.

As shown in Figure 4-23, there are two commands: register read and register write. Figure 4-11 and Figure 4-12 show the timing for these two operations.

TABLE 4-23: REGISTER ACCESS USING THE SPI INTERFACE

SPI Operation	Command/Address Phase (SDI pin)		TA bits (Note 4-8)	Data Phase (SDO or SDI pins)
	Command	Register Address		
Register Read	011	A23 A22 A21 A20 … A7 A6 A5 A4 A3 A2 A1 A0	XXXXX	D7 D6 D5 D4 D3 D2 D1 D0
Register Write	010	A23 A22 A21 A20 … A7 A6 A5 A4 A3 A2 A1 A0	XXXXX	D7 D6 D5 D4 D3 D2 D1 D0

Note 4-8 TA bits are turn-around bits. They are “don't care” bits.

Note: The actual device address space is 16 bits (A15 - A0), so the values of address bits A23 - A16 in the SPI command/address phase are “don't care”.

FIGURE 4-11: SPI REGISTER READ OPERATION

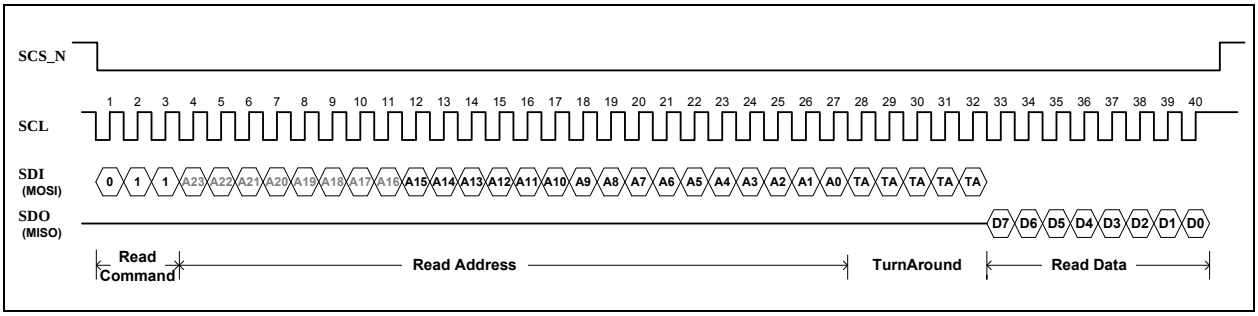
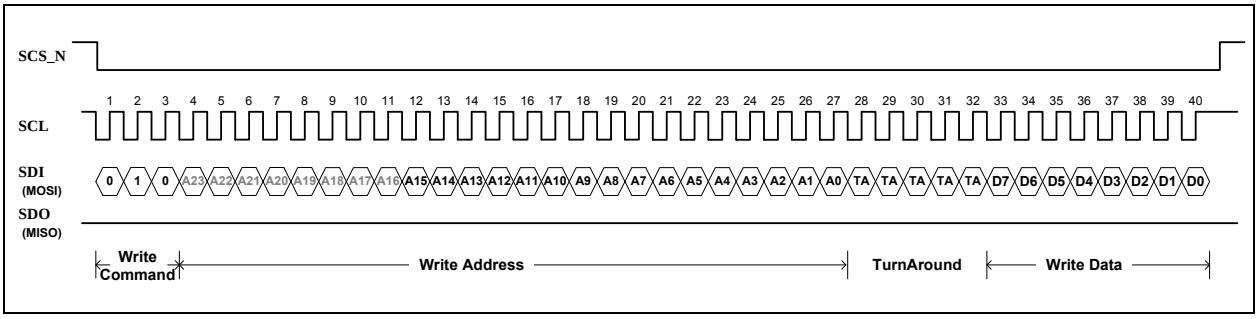


FIGURE 4-12: SPI REGISTER WRITE OPERATION



4.11.2 I²C BUS

The management interface may be configured to be an I²C slave. In this mode, an I²C master has complete programming access to the device's internal control and status registers, including all MIB counters, address lookup tables, VLAN table and ACL table.

The 7-bit device address is fixed as 1011_111. Because of the fixed address, only one KSZ8567R may be on the I²C bus at a time. The R/W control bit is then appended as the least significant bit to form these 8-bit address/control words:

1011_1110 <write>

1011_1111 <read>

The internal registers and tables of the device are accessed using 16-bit addressing and 8-bit data. The access formats are as follows:

FIGURE 4-13: SINGLE BYTE REGISTER WRITE

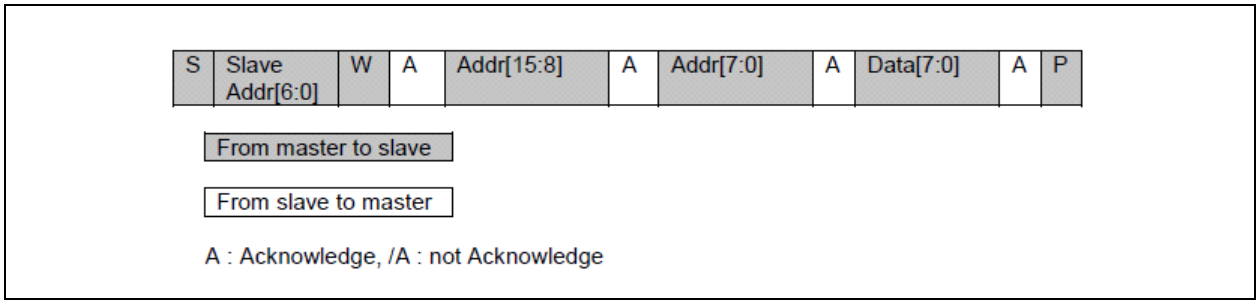


FIGURE 4-14: SINGLE BYTE REGISTER READ

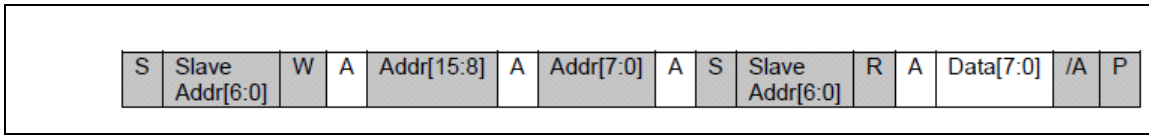


FIGURE 4-15: BURST REGISTER WRITE

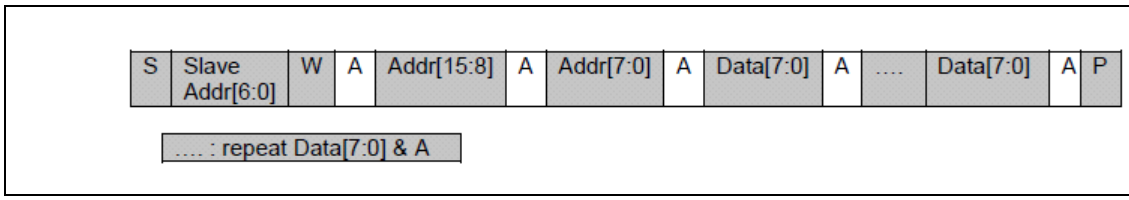
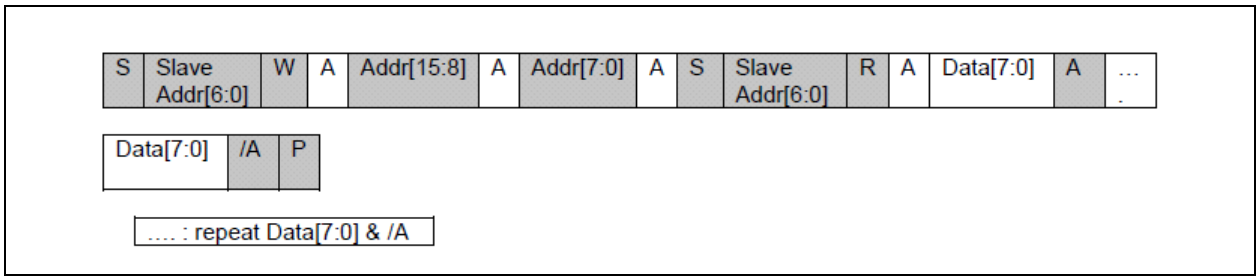


FIGURE 4-16: BURST REGISTER READ



4.11.3 MII MANAGEMENT (MIIM) INTERFACE

The device supports the IEEE 802.3 MII management interface, also known as the management data input/output (MDIO) interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8567R PHY blocks, but it does not provide access to the switch registers. An external device with MDC/MDIO capability can read the PHY status or configure the PHY settings. Details on the MIIM interface can be found in Clauses 22 and 45 of the IEEE 802.3 Specification.

Use of MIIM conflicts with use of the In-Band Management interface. These interfaces cannot be used simultaneously.

The MIIM interface consists of the following:

- A physical connection that uses a data signal (**MDIO**) and a clock signal (**MDC**) for communication between an external controller and the KSZ8567R. Note that the **MDIO** signal is open-drain.
- A specific protocol that operates across the two signal physical connection that allows an external controller to communicate with the internal PHY devices.
- Access to a set of standard, vendor-specific and extended (MMD) 16-bit registers. These registers are also directly accessible via the SPI and I^2C interface options.

The MIIM Interface can operate up to a maximum clock speed of 5MHz. Access is limited to only the registers in the PHY blocks of ports 1 through 5. Table 4-24 summarizes the MII management interface frame format.

TABLE 4-24: MII MANAGEMENT INTERFACE FRAME FORMAT

Operation Mode	Preamble (32-bit)	Start of Frame (2-bit)	Operation Code (2-bit)	PHY Address (5-bit)	Register Address (5-bit)	Turn Around (2-bit)	Register Data (16-bit)	Idle
Read	All 1s	01	10	A[4:0]	Reg[4:0]	Z0	D[15:0]	Z
Write	All 1s	01	01	A[4:0]	Reg[4:0]	10	D[15:0]	Z

The MIIM PHY address to PHY port mapping is as follows:

- PHY Address 1h to PHY port 1
- PHY Address 2h to PHY port 2
- PHY Address 3h to PHY port 3
- PHY Address 4h to PHY port 4
- PHY Address 5h to PHY port 5

The MIIM register address space consists of two distinct areas.

- Standard MIIM Registers (Direct)
- MDIO Manageable Device (MMD) Registers (Indirect)

4.11.3.1 Standard MIIM Registers (Direct)

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0h to Fh) are defined according to the IEEE specification, while the remaining 16 registers (Registers 10h to 1Fh) are defined specific to the PHY vendor.

The KSZ8567R supports the standard registers listed in Table 4-25 for each PHY port. Each 16-bit MIIM Standard Register Address maps to two corresponding 8-bit Port N Register Addresses. The register bit map and description are located at the 8-bit Port N Register Addresses.

TABLE 4-25: STANDARD MIIM REGISTERS

MIIM Standard Register Address (hex)	Port N Register Address (hex)	Description
IEEE-Defined Registers		
0h	0xN100 - 0xN101	PHY Basic Control Register
1h	0xN102 - 0xN103	PHY Basic Status Register
2h	0xN104 - 0xN105	PHY ID High Register

TABLE 4-25: STANDARD MIIM REGISTERS (CONTINUED)

MIIM Standard Register Address (hex)	Port N Register Address (hex)	Description
3h	0xN106 - 0xN107	PHY ID Low Register
4h	0xN108 - 0xN109	PHY Auto-Negotiation Advertisement Register
5h	0xN10A - 0xN10B	PHY Auto-Negotiation Link Partner Ability Register
6h	0xN10C - 0xN10D	PHY Auto-Negotiation Expansion Status Register
7h	0xN10E - 0xN10F	PHY Auto-Negotiation Next Page Register
8h	0xN110 - 0xN111	PHY Auto-Negotiation Link Partner Next Page Ability Register
9h-Ch	-	RESERVED
Dh	0xN11A - 0xN11B	PHY MMD Setup Register
Eh	0xN11C - 0xN11D	PHY MMD Data Register
Fh	-	RESERVED
Vendor-Specific Registers		
10h	-	RESERVED
11h	0xN122 - 0xN123	PHY Remote Loopback Register
12h	0xN124 - 0xN125	PHY LinkMD Register
13h	0xN126 - 0xN127	PHY Digital PMA/PCS Status Register
14h	-	RESERVED
15h	0xN12A - 0xN12B	Port RXER Count Register
16h-1Ah	-	RESERVED
1Bh	0xN136 - 0xN137	Port Interrupt Control / Status Register
1Ch	0xN138 - 0xN139	PHY Auto MDI / MDI-X Register
1Dh-1Eh	-	RESERVED
1Fh	0xN13E - 0xN13F	PHY Control Register

4.11.3.2 MDIO Manageable Device (MMD) Registers (Indirect)

The MIIM interface provides indirect access to a set of MMD registers as defined in Section 5.4, "MDIO Manageable Device (MMD) Registers (Indirect)," on page 195.

4.12 In-Band Management

The in-band management access (IBA) is a feature that provides full register read and write access via any one of the seven data ports. Port 7 is the default IBA port. The in-band feature is enabled or disabled by a strapping option at power-up and reset. To use a different port instead of port 7 for IBA, the SPI or I^2C interface or IBA must be used to write to a control register. IBA may not be used on more than one port at a time.

In-band management frames are processed differently from normal network frames. They are recognized as special frames, so address and VID lookup, VLAN tagging, source address filtering, un-tag discard, tagged frame drop, etc. are not applied to them. Received in-band management frames are never forwarded to the switch fabric or to any other port.

The In-Band Management (IBA) Control Register is used to enable and control the IBA feature and to specify one of the seven ports as the IBA port.

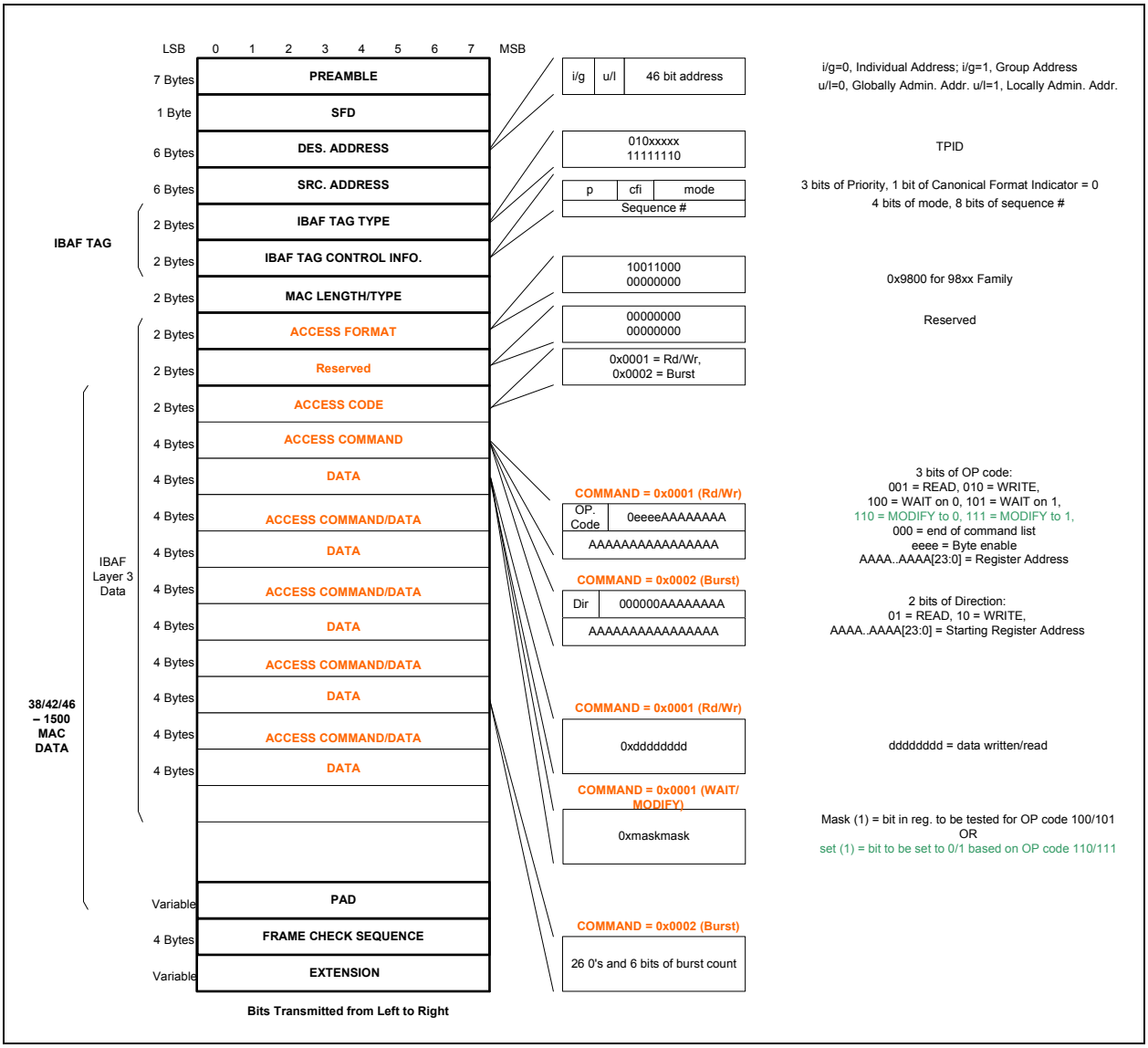
The IBA frame format is shown in Figure 4-17. The layer 2 portion of the IBA frame contains normal destination address (DA) and source address (SA) fields. The DA of the frames are defined to be the switch MAC address (default 00-10-A1-FF-FF-FF), and the SA is the MAC address of the source device. The DA and SA will be swapped in the response frame. A special 4-byte IBA tag follows the SA. This is then followed by the 2-byte EtherType/Length field that serves to identify this as an IBA frame.

Only one IBA frame can be processed at a time. Any subsequent IBA frames received by the device will be dropped unless the most recent response frame has been fully transmitted.

There are six types of read/write commands: READ, WRITE, WAIT on 0, WAIT on 1, MODIFY to 0 and MODIFY to 1.

The burst commands offer fast and bundled data return, up to the capacity of the IBA frame buffer. There are two types of operations in burst command: READ burst and Write burst.

FIGURE 4-17: IN-BAND MANAGEMENT FRAME FORMAT



4.13 MAC Interface (RGMII/MII/RMII Port 6-7)

Strapping options are used to individually select any of these MAC interface options for ports 6 and 7:

- Media Independent Interface (MII): Supports 100 and 10 Mbps data rates
- Reduced Media Independent Interface (RMII): Supports 100 and 10 Mbps data rates
- Reduced Gigabit Media Independent Interface (RGMII): Supports 1000, 100 and 10 Mbps data rates

Note that the signals on the KSZ8567R MAC interfaces are named as they would be for a PHY: the TX direction is into the KSZ8567R, while the RX direction is out of the KSZ8567R, as if to a host processor with integrated MAC. Signal connection to such a “MAC” device is TX-to-TX, and RX-to-RX.

An external PHY (such as the Microchip KSZ9031RNX) may be connected to either port, but in that case the signal connection will be RX-to-TX, and TX-to-RX.

The RGMII/MII/RMII interfaces are powered by the **VDDIO** power supply.

4.13.1 MEDIA INDEPENDENT INTERFACE (MII)

The media independent interface (MII) is specified in Clause 22 of the IEEE 802.3 standard. It provides a common interface between PHY layer and MAC layer devices. The data interface is 4-bits wide and runs at one quarter the network bit rate; either 2.5MHz in 10BASE-T/Te or 25MHz in 100BASE-TX (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Similarly, the receive side provides signals that convey when the data is valid and without physical layer errors. For half duplex operation, the COL signal indicates if a collision has occurred during transmission.

Each MII interface operates in either PHY Mode or MAC Mode. Select PHY Mode when the port is connected to a processor or other device with a MAC function; select MAC Mode when connecting to an external PHY. Note that the direction of the **TX_CLK*x***, **RX_CLK*x***, **COL*x*** and **CRS*x*** signals is affected by the PHY mode or MAC mode setting, while other MII signals do not change direction.

MII mode is selected at reset by a configuration strap option on pins **RXD6_3** and **RXD6_2** for port 6, and pins **RXD7_3** and **RXD7_2** for port 7. The Speed strapping option (on pin **RXD6_0** for port 6 and **RXD7_0** for port 7) should be set for 100/10 Mbps Mode. PHY Mode or MAC Mode is selected by strapping option on pins **RXD6_1** (port 6) and **RXD7_1** (port 7). Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

The interface contains two distinct groups of signals, one for transmission and the other for reception. Table 4-26 and Table 4-27 describe the signals used by the MII interface to connect to an external MAC or to an external PHY, respectively.

TABLE 4-26: MII (PHY MODE) CONNECTION TO EXTERNAL MAC

MII Interface Signals Description	KSZ8567R Signals in PHY Mode	External MAC Device Signals
Transmit Enable	**TX_EN*x*** (input)	TX_EN (output)
Transit Error	**TX_ER*x*** (input)	TX_ER (output)
Transmit Data Bits [3:0]	**TXD*x*_[3:0]** (input)	TXD[3:0] (output)
Transmit Clock	**TX_CLK*x*** (output)	TX_CLK (input)
Collision Detection	**COL*x*** (output)	COL (input)
Carrier Sense	**CRS*x*** (output)	CRS (input)
Received Data Valid	**RX_DV*x*** (output)	RX_DV (input)
Receive Error	**RX_ER*x*** (output)	RX_ER (input)
Receive Data Bits [3:0]	**RXD*x*_[3:0]** (output)	RXD[3:0] (input)
Receive Clock	**RX_CLK*x*** (output)	RX_CLK (input)

TABLE 4-27: MII (MAC MODE) CONNECTION TO EXTERNAL PHY

MII Interface Signals Description	KSZ8567R Signals in MAC Mode	External PHY Device Signals
Transmit Enable	**RX_DV*x*** (output)	TX_EN (input)
Transit Error	**RX_ER*x*** (output)	TX_ER (input)
Transmit Data Bits [3:0]	**RXD*x*_[3:0]** (output)	TXD[3:0] (input)
Transmit Clock	**RX_CLK*x*** (input)	TX_CLK (output)
Collision Detection	**COL*x*** (input)	COL (output)
Carrier Sense	**CRS*x*** (input)	CRS (output)
Received Data Valid	**TX_EN*x*** (input)	RX_DV (output)
Receive Error	**TX_ER*x*** (input)	RX_ER (output)

TABLE 4-27: MII (MAC MODE) CONNECTION TO EXTERNAL PHY (CONTINUED)

MII Interface Signals Description	KSZ8567R Signals in MAC Mode	External PHY Device Signals
Receive Data Bits [3:0]	**TXD*x*_[3:0]** (input)	RXD[3:0] (output)
Receive Clock	**TX_CLK*x*** (input)	RX_CLK (output)

4.13.2 REDUCED MEDIA INDEPENDENT INTERFACE (RMII)

The reduced media independent interface (RMII) specifies a low pin count interface, which is based on MII, that provides communication with a MAC attached to the port. As with MII, RMII provides a common interface between physical layer and MAC layer devices, or between two MAC layer devices, and has the following key characteristics:

- Supports network data rates of either 10Mbps or 100Mbps.
- Uses a single 50MHz clock reference (provided internally or externally) for both transmit and receive data.
- Uses independent 2-bit wide transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The user selects one of the two RMII clocking modes by setting the appropriate strapping option. The clocking mode is selected separately for ports 6 and 7.

While in RMII Normal Mode, the port will require an external 50MHz signal to be input to **TX_CLK*x*/REFCLKI*x*** from an external source. This mode is selected by strapping the appropriate pin (**RXD6_1** for port 6; **RXD7_1** for port 7) high during reset.

While in RMII Clock Mode, the port will output a 50MHz clock on **RX_CLK*x*/REFCLKO*x***, which is derived from the 25MHz crystal or oscillator attached to the **XI** clock input. The **TX_CLK*x*/REFCLKI*x*** input is unused in this mode. This mode is selected by strapping the appropriate pin (**RXD6_1** for port 6; **RXD7_1** for port 7) low during reset.

Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional configuration strap information.

Table 4-28 describes the signals used by the RMII interface. Refer to the RMII specification for full details on the signal descriptions.

TABLE 4-28: RMII SIGNAL DESCRIPTIONS

RMII Signal Name (per spec)	RMII Signal (per KSZ8567R)	Pin Direction (with respect to PHY, KSZ8567R)	Pin Direction (with respect to MAC)	RMII Signal Description
REF_CLK	**REFCLKI6** **REFCLKI7**	Input	Input or Output	Synchronous 50MHz reference clock, when port is in RMII Normal Mode
n/a	**REFCLKO6** **REFCLKO7**	Output	Input	Synchronous 50MHz reference clock, when port is in RMII Clock Mode
TX_EN	**TX_EN6** **TX_EN7**	Input	Output	Transmit Enable
TXD[1:0]	**TXD6_[1:0]** **TXD7_[1:0]**	Input	Output	Transmit Data Bit [1:0]
CRS_DV	**RX_DV6** **RX_DV7**	Output	Input	Carrier Sense / Receive Data Valid
RX_ER	**RX_ER6** **RX_ER7**	Output	Input or not required	Receive Error
RXD[1:0]	**RXD6_[1:0]** **RXD7_[1:0]**	Output	Input	Receive Data Bit [1:0]

A device port in RMII mode may connect to either an external MAC device (such as a host processor) or to an external PHY; but unlike MII, RMII does not provide separate PHY and MAC modes of operation. However, it is necessary to connect the pins properly.

TABLE 4-29: RMII CONNECTION TO EXTERNAL MAC

RMII Interface Signals Description	KSZ8567R Signals	External MAC Device Signals
Transmit Enable	**TX_EN*x*** (input)	TX_EN (output)
Transmit Data Bits [1:0]	**TXD*x*_[1:0]** (input)	TXD[1:0] (output)
Reference Clock	**REFCLKI*x*** (input) or **REFCLKO*x*** (output)	REF_CLK (input or output)
Carrier Sense Data Valid	**RX_DV*x*** (output)	CRS_DV (input)
Receive Error	**RX_ER*x*** (output)	RX_ER (input)
Receive Data Bits [1:0]	**RXD*x*_[1:0]** (output)	RXD[1:0] (input)

TABLE 4-30: RMII CONNECTION TO EXTERNAL PHY

RMII Interface Signals Description	KSZ8567R Signals	External PHY Device Signals
Transmit Enable	**RX_DV*x*** (output)	TX_EN (input)
Transmit Data Bits [1:0]	**RXD*x*_[1:0]** (output)	TXD[1:0] (input)
Reference Clock	**REFCLKI*x*** (input) or **REFCLKO*x*** (output)	REF_CLK (input or output)
Carrier Sense Data Valid	**TX_EN*x*** (input)	CRS_DV (output)
Receive Error	No connection	RX_ER (output)
Receive Data Bits [1:0]	**TXD*x*_[1:0]** (input)	RXD[1:0] (output)

4.13.3 REDUCED GIGABIT MEDIA INDEPENDENT INTERFACE (RGMII)

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for GMII to 12 pins for RGMII.
- All speeds (10Mbps, 100Mbps and 1000Mbps) are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each four bits wide - a nibble.

In RGMII operation, the RGMII pins function as follows:

- The MAC sources the transmit reference clock, **TX_CLK*x***, at 125MHz for 1000Mbps, 25MHz for 100Mbps, and 2.5MHz for 10Mbps.
- The PHY recovers and sources the receive reference clock, **RX_CLK*x***, at 125MHz for 1000Mbps, 25MHz for 100Mbps, and 2.5MHz for 10Mbps.
- For 1000BASE-T, the transmit data, **TXD*x*_[3:0]**, is presented on both edges of **TX_CLK*x***, and the received data, **RXD*x*_[3:0]**, is clocked out on both edges of the recovered 125MHz clock, **RX_CLK*x***.
- For 10BASE-T/100BASE-TX, the MAC holds **TX_CTL*x*** low until both the PHY and MAC operate at the same speed. During the speed transition, the receive clock is stretched on either a positive of neagative pulse to ensure that no clock glitch is presented to the MAC.
- **TX_ER*x*** and **RX_ER*x*** are combined with **TX_EN*x*** and **RX_DV*x***, respectively, to form **TX_CTL*x*** and **RX_CTL*x***. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the device is configured to RGMII mode if the appropriate configuration strap pins are set to one of the RGMII mode capability options. Refer to Section 3.2.1, "Configuration Straps," on page 16 for available options. Note that there is no mechanism for the RGMII interface to adapt its speed automatically to the speed of the connected RGMII device. A configuration strap option sets the speed of each RGMII interface at power-up to either 1000Mbps or 100Mbps. For each port, a control register can override the configuration strap option and set the RGMII speed to either 1000, 100 or 10Mbps. If a PHY is connected to an RGMII port, it should be ensured that the PHY link speed is fixed in order to avoid a mismatch to the RGMII speed.

The device provides the option to add a minimum of 1.5ns internal delay to either **TX_CLK*x*** or **RX_CLK*x***, via the RGMII Internal Delay control bits in the XMII Port Control 1 Register. This can reduce or eliminate the need to add trace delay to the clock signals on the printed circuit board. RGMII_ID_ig enables delay on **TX_CLK*x***, and the default is off. RGMII_ID_eg enables delay on **RX_CLK*x***, and the default is on. Users should also be aware of any internal clock delay that may be added by the connected RGMII device.

TABLE 4-31: RGMII SIGNAL DESCRIPTIONS

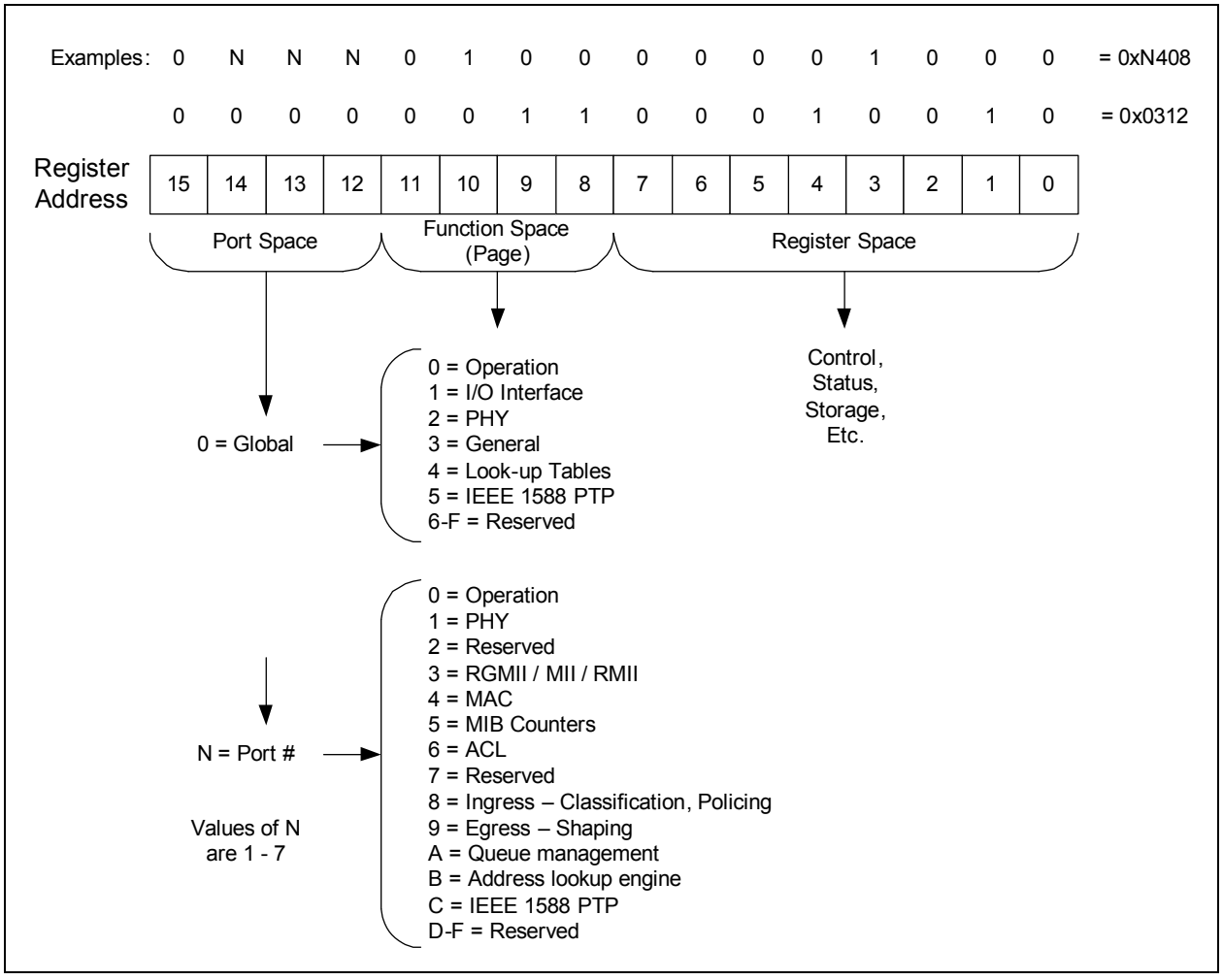
RGMII Signal Name (per spec)	RGMII Signal (per KSZ8567R)	Pin Direction (with respect to PHY, KSZ8567R)	Pin Direction (with respect to MAC)	RGMII Signal Description
TXC	**TX_CLK6** **TX_CLK7**	Input	Output	Transmit Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
TX_CTL	**TX_CTL6** **TX_CTL7**	Input	Output	Transmit Control
TXD[3:0]	**TXD6_[3:0]** **TXD7_[3:0]**	Input	Output	Transmit Data [3:0]
RXC	**RX_CLK6** **RX_CLK7**	Output	Input	Receive Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
RX_CTL	**RX_CTL6** **RX_CTL7**	Output	Input	Receive Control
RXD[3:0]	**RXD6_[3:0]** **RXD7_[3:0]**	Output	Input	Receive Data [3:0]

5.0 DEVICE REGISTERS

The KSZ8567R has a rich set of registers for device management. The registers are accessed by the SPI or I^2C interfaces, or by in-band management. Alternatively, the MIIM interface can be used to access the PHY registers only. The MIIM interface cannot access the switch registers.

A 16-bit address is used to access the device registers. This address is split into three hierarchical spaces, as shown in Figure 5-1. These three spaces are used to designate the port/channel (4-bits), function (page) of the port (4-bits), and register of function (8-bits). The individual ports are numbered 1 through 7. In the port space, a value of 0 is used for global registers. Address bit 15 is always 0.

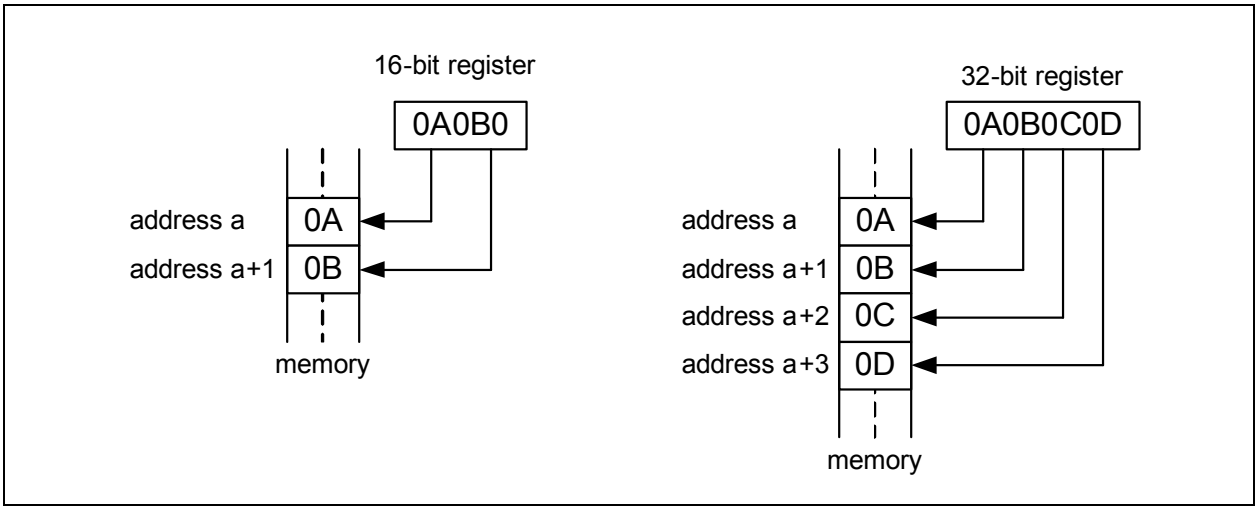
FIGURE 5-1: REGISTER ADDRESS MAPPING



Register addressing is by bytes, and the management interface (SPI, I^2C or in-band) transfers data by bytes. Where registers are shown as 16-bits or 32-bits, this is for descriptive purposes only. Data can always be written and read as individual bytes and in any order.

For multi-byte registers, the data is addressed in a big-endian format, with the most significant byte at the lowest address, and the least significant byte at the highest address, as shown in Figure 5-2.

FIGURE 5-2: BYTE ORDERING



The global and port register address maps are detailed in Table 5-1 and Table 5-2, respectively. Table 1-3, “Register Nomenclature,” on page 7 provides a list of register bit type notations.

The remainder of this chapter is organized as follows:

- Global Registers
- Port Registers
- Tables and MIB Counters (Access)
- MDIO Manageable Device (MMD) Registers (Indirect)

TABLE 5-1: GLOBAL REGISTER ADDRESS MAP

Address	Functional Group
0x0000 - 0x00FF	Global Operation Control Registers (0x0000 - 0x00FF)
0x0100 - 0x01FF	Global I/O Control Registers (0x0100 - 0x01FF)
0x0200 - 0x02FF	Global PHY Control and Status Registers (0x0200 - 0x02FF)
0x0300 - 0x03FF	Global Switch Control Registers (0x0300 - 0x03FF)
0x0400 - 0x04FF	Global Switch Look Up Engine (LUE) Control Registers (0x0400 - 0x04FF)
0x0500 - 0x05FF	Global Switch PTP Control Registers (0x0500 - 0x05FF)
0x0600 - 0x0FFF	RESERVED

TABLE 5-2: PORT N (1-7) REGISTER ADDRESS MAP

Address	Functional Group
0xN000 - 0xN0FF	Port N: Port Operation Control Registers (0xN000 - 0xN0FF)
0xN100 - 0xN1FF	Port N: Port Ethernet PHY Registers (0xN100 - 0xN1FF)
0xN200 - 0xN2FF	RESERVED
0xN300 - 0xN3FF	Port N: Port RGMII/MII/RMII Control Registers (0xN300 - 0xN3FF)
0xN400 - 0xN4FF	Port N: Port Switch MAC Control Registers (0xN400 - 0xN4FF)
0xN500 - 0xN5FF	Port N: Port Switch MIB Counters Registers (0xN500 - 0xN5FF)
0xN600 - 0xN6FF	Port N: Port Switch ACL Control Registers (0xN600 - 0xN6FF)
0xN700 - 0xN7FF	RESERVED
0xN800 - 0xN8FF	Port N: Port Switch Ingress Control Registers (0xN800 - 0xN8FF)
0xN900 - 0xN9FF	Port N: Port Switch Egress Control Registers (0xN900 - 0xN9FF)
0xNA00 - 0xNAFF	Port N: Port Switch Queue Management Control Registers (0xNA00 - 0xNAFF)
0xNB00 - 0xNBFF	Port N: Port Switch Address Lookup Control Registers (0xNB00 - 0xNBFF)
0xNC00 - 0xNCFF	Port N: Port Switch PTP Control Registers (0xNC00 - 0xNCFF)
0xND00 - 0xNFFF	RESERVED

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results. If it is necessary to write to registers which contain both writable and reserved bits in the same register, the user should first read back the reserved bits (RO or R/W), "OR" the desired settable bits with the value read, and then write back the "ORed" value to the register.

5.1 Global Registers

This section details the device's global registers. For an overview of the device's entire register map, refer to Section 5.0, "Device Registers". For details on the device's port registers, refer to Section 5.2, "Port Registers".

5.1.1 GLOBAL OPERATION CONTROL REGISTERS (0x0000 - 0x00FF)

5.1.1.1 Global Chip ID 0 Register

Address: 0x0000 Size: 8 bits

Bits	Description	Type	Default
7:0	**Fixed Value**	RO	0x00

5.1.1.2 Global Chip ID 1 Register

Address: 0x0001 Size: 8 bits

Bits	Description	Type	Default
7:0	**Chip ID (MSB)**	RO	0x85

5.1.1.3 Global Chip ID 2 Register

Address: 0x0002 Size: 8 bits

Bits	Description	Type	Default
7:0	**Chip ID (LSB)**	RO	0x67

5.1.1.4 Global Chip ID 3 Register

Address: 0x0003 Size: 8 bits

Bits	Description	Type	Default
7:4	**Revision ID**	RO	-
3:1	**RESERVED**	RO	-
0	**Global Software Reset** Refer to the Switch Operation Register for another reset control bit. 0 = Normal operation 1 = Resets the data path and state machines, but not register values.	R/W SC	0b

5.1.1.5 PME Pin Control Register

Address: 0x0006 Size: 8 bits

Bits	Description	Type	Default
7:2	**RESERVED**	RO	-
1	**PME Pin Output Enable** 0 = Disabled 1 = Enabled	R/W	0b
0	**PME Pin Output Polarity** 0 = PME is active low 1 = PME is active high	R/W	0b

5.1.1.6 Global Interrupt Status Register

Address: 0x0010 - 0x0013 Size: 32 bits

This register provides the top level interrupt status for the LUE and GPIO trigger and timestamp functions. These interrupts are enabled in the Global Interrupt Mask Register. For port specific interrupts, refer to the Port Interrupt Status Register.

Bits	Description	Type	Default
31	**Lookup Engine (LUE) Interrupt Status** Refer to the Address Lookup Table Interrupt Register for detailed LUE interrupt status bits. 0 = No interrupt 1 = Interrupt request	RO	0b
30	**GPIO Pin Output Trigger and Timestamp Unit Interrupt Status** Refer to the GPIO Status Monitor 1 Register to determine whether it is a Trigger Output Unit interrupt or a Timestamp Unit interrupt. For the interrupt status for the port-based time stamping of PTP egress frames, refer to the Port Interrupt Status Register and Port PTP Timestamp Interrupt Status Register. 0 = No interrupt 1 = Interrupt request	RO	0b
29:0	**RESERVED**	RO	-

5.1.1.7 Global Interrupt Mask Register

Address: 0x0014 - 0x0017 Size: 32 bits

This register enables the interrupts in the Global Interrupt Status Register.

Bits	Description	Type	Default
31	**Lookup Engine (LUE) Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
30	**GPIO Pin Output Trigger and Timestamp Unit Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
29:0	**RESERVED**	RO	-

5.1.1.8 Global Port Interrupt Status Register

Address: 0x0018 - 0x001B Size: 32 bits

This register provides the top level interrupt status for the individual ports. These interrupts are enabled in the Global Port Interrupt Mask Register. Refer to the Port Interrupt Status Register for detailed port interrupt status.

Bits	Description	Type	Default
31:7	**RESERVED**	RO	-
6	**Port 7 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
5	**Port 6 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
4	**Port 5 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
3	**Port 4 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
2	**Port 3 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
1	**Port 2 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b
0	**Port 1 Interrupt Status** 0 = No interrupt 1 = Interrupt request	RO	0b

5.1.1.9 Global Port Interrupt Mask Register

Address: 0x001C - 0x001F Size: 32 bits

This register enables the interrupts in the Global Port Interrupt Status Register.

Bits	Description	Type	Default
31:7	**RESERVED**	RO	-
6	**Port 7 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
5	**Port 6 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
4	**Port 5 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
3	**Port 4 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
2	**Port 3 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
1	**Port 2 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
0	**Port 1 Interrupt Mask** 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b

5.1.2 GLOBAL I/O CONTROL REGISTERS (0x0100 - 0x01FF)

5.1.2.1 Serial I/O Control Register

Address: 0x0100 Size: 8 bits

Bits	Description	Type	Default
7:3	**RESERVED**	R/W	0100_0b
2	**MIIM Preamble Suppression** This feature affects only the MIIM (MDIO / MDC) interface. When using SPI or I^2C, this bit has no effect. 0 = Normal operation. The switch always expects the MIIM preamble. 1 = The switch will respond to MIIM commands even in the absence of a preamble.	R/W	0b
1	**Automatic SPI Data Out Edge Select** When enabled, this feature automatically determines the edge of **SCL** that is used to clock out the SPI data on **SDO**. If **SCL** ≥ ~25MHz, **SDO** data is clocked by the rising edge of **SCL**. If **SCL** < ~25 MHz, **SDO** data is clocked by the falling edge of **SCL**. 0 = The automatic feature is disabled, and bit 0 determines the SCL clock edge used for SDO. 1 = The automatic feature is enabled, and bit 0 is ignored.	R/W	1b
0	**SPI Data Out Edge Select** When bit 1 is zero, then this bit determines the clock edge used for SPI data out. When bit 1 is set to 1, this bit is ignored. 0 = **SDO** data is clocked by the falling edge of **SCL** 1 = **SDO** data is clocked by the rising edge of **SCL**	R/W	0b

5.1.2.2 Output Clock Control Register

Address: 0x0103 Size: 8 bits

Bits	Description	Type	Default
7	**Recovered Clock Ready (REC_CLK_RDY)** 0 = The selected recovered clock is not ready 1 = The selected recovered clock is ready	RO	-
6:5	**RESERVED**	RO	00b
4:2	**SYNCLKO Source** 000 = From crystal / clock input at **XI** pin 001 = From port 1 recovered clock 010 = From port 2 recovered clock 011 = From port 3 recovered clock 100 = From port 4 recovered clock 101 = From port 5 recovered clock 110 – 111 = Reserved	R/W	000b

Bits	Description	Type	Default
1	**SYNCLKO Output Pin Enable** 0 = Disabled 1 = Enabled	R/W	1b
0	**SYNCLKO Frequency** 0 = 25 MHz 1 = 125 MHz	R/W	0b

5.1.2.3 In-Band Management (IBA) Control Register

Address: 0x0104 - 0x0107 Size: 32 bits

This register controls the In-Band Access (IBA) feature.

Bits	Description	Type	Default
31	**IBA Enable** The initial value is strapped in from the **RX_DV7/CRS_DV7/RX_CTL7** pin. 0 = Disabled 1 = Enabled	R/W	Note 5-1
30	**IBA Destination MAC Address Match Enable** Set this bit to enable checking of the destination MAC address in received IBA frames against the switch MAC address in the Switch MAC Address 0 Register through Switch MAC Address 5 Register. Non-matching frames are discarded. When not enabled, the MAC address is not checked.	R/W	0b
29	**IBA Reset** Set this bit to initialize the IBA state machine. This bit is self-clearing.	R/W SC	0b
28:24	**RESERVED**	RO	0x00
23:22	**Priority Queue for IBA response** Specifies the transmit priority queue for the IBA response frame. Typically this value is not changed.	R/W	01b
21:19	**RESERVED**	RO	00_0b
18:16	**Port used for IBA communication** 000 = Port 1 001 = Port 2 010 = Port 3 011 = Port 4 100 = Port 5 101 = Port 6 110 = Port 7 111 = Reserved	R/W	110
15:0	**TPID (EtherType) value for IBA frame header**	R/W	0x40FE

Note 5-1 The default value of this field is determined by the associated configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.1.2.4 I/O Drive Strength Register

Address: 0x010D Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	R/W	0b
6:4	**High Speed Drive Strength (24mA)** Controls drive strength of RGMII / MII / RMII (except **TX_CLK** / **REFCLKI**, **COL** and **CRS**) and **SYNCLKO**.	R/W	110b
3	**RESERVED**	R/W	0b
2:0	**Low Speed Drive Strength (8mA)** Controls drive strength of **TX_CLK** / **REFCLKI**, **COL**, **CRS**, LEDs, **PME_N**, **INTRP_N**, **SDO** and **SDI/SDA/MDIO**.	R/W	10b

5.1.2.5 In-Band Management (IBA) Operation Status 1 Register

Address: 0x0110 - 0x0113 Size: 32 bits

Bits	Description	Type	Default
31	**Good IBA Packet Detect** 1 = A good IBA packet is received.	RO	0b
30	**IBA Response Packet Transmit Done** 1 = An IBA response packet is sent out. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
29	**IBA Execution Done** 1 = All the commands in one IBA packet are completely executed. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
28:15	**RESERVED**	RO	0x0000
14	**IBA MAC Address Mismatch Error** This bit is active only when IBA_ENABLE (In-Band Management (IBA) Control Register, bit 30) is set. 1 = An IBA packet is received with an unmatched MAC address, unequal to the switch's MAC address. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
13	**IBA Access Format Error** 1 = An IBA packet with a wrong access format (not equal to 0x9800) is received. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
12	**IBA Access Code Error** 1 = An IBA packet with an unrecognized access code is received. (Valid access codes are 0x0001 and 0x0002.) This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b

Bits	Description	Type	Default
11	**IBA Access Command Error** 1 = An IBA packet with an unrecognized command code is received. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
10	**IBA Oversize Packet Error** 1 = An oversized IBA packet is received. The maximum IBA packet size is 320 bytes, including 8-byte zeros before FCS and the 4-byte FCS. No response packet is sent. This bit is cleared when a packet with a matching IBA tag field is received.	RO	0b
9:7	**RESERVED**	RO	000b
6:0	**IBA Access Code Error Location** When IBA Access Command Error (bit 11) is set, these bits indicate the address location of the wrong command code within the IBA packet.	RO	0x000

5.1.2.6 LED Override Register

Address: 0x0120 - 0x0123 Size: 32 bits

Bits	Description	Type	Default
31:10	**RESERVED**	RO	0x00000
9:0	**Override LED** These bits select whether each **LEDx_0** and **LEDx_1** pin will function as an LED or General Purpose Output (GPO). The LSB bit of this field represents **LED1_0**, followed by **LED1_1**, **LED2_0**, etc.. When configured as a GPO, the GPO output is controlled via the LED Output Register. 0 = **LEDx_y** pin functions as an LED 1 = **LEDx_y** pin functions as a GPO		0000000000b

5.1.2.7 LED Output Register

Address: 0x0124 - 0x0127 Size: 32 bits

Bits	Description	Type	Default
31:10	**RESERVED**	RO	0x00000
9:0	**GPO Output Control** When configured as a GPO via the LED Override Register, the GPO output is controlled via this field. The LSB bit of this field represents **LED1_0**, followed by **LED1_1**, **LED2_0**, etc.. 0 = **LEDx_y** pin outputs low 1 = **LEDx_y** pin outputs high	R/W	0000000000b

5.1.2.8 LED2_0/LED2_1 Source Register

Address: 0x0128 - 0x012B Size: 32 bits

Bits	Description	Type	Default
31:4	**RESERVED**	RO	0x0000000
3	**LED2_1 Source** 0 = **LED2_1** outputs as LED/GPO (configured via the LED Override Register) 1 = **LED2_1** outputs the PTP Trigger Output 1	R/W	0b
2	**LED2_0 Source** 0 = **LED2_0** outputs as LED/GPO (configured via the LED Override Register) 1 = **LED2_0** outputs the PTP Trigger Output 0	R/W	0b
1:0	**RESERVED**	RO	00b

5.1.3 GLOBAL PHY CONTROL AND STATUS REGISTERS (0x0200 - 0x02FF)

5.1.3.1 Power Down Control 0 Register

Address: 0x0201 Size: 8 bits

Bits	Description	Type	Default
7:6	**RESERVED**	RO	00b
5	**PLL Power Down** 0 = Normal operation. 1 = Disable PLL. This may be used in combination with EDPD mode – see below.	R/W	0b
4:3	**Power Management Mode** 00 = Normal operation 01 = Energy Detect Power Down (EDPD) Mode 10 = Soft Power Down Mode 11 = invalid	R/W	00b
2:0	**RESERVED**	RO	000b

5.1.3.2 LED Configuration Strap Register

Address: 0x0210 - 0x0213 Size: 32 bits

Bits	Description	Type	Default
31:10	**RESERVED**	RO	0x000000
9:0	**Configuration strap values of LED pins** **[LED4_1, LED4_0, LED3_1, LED3_0, LED2_1, LED2_0, LED1_1, LED1_0]**	RO	Note 5-2

Note 5-2 The default value of this field is determined by the associated configuration strap values. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.1.4 GLOBAL SWITCH CONTROL REGISTERS (0x0300 - 0x03FF)

5.1.4.1 Switch Operation Register

Address: 0x0300 Size: 8 bits

Bits	Description	Type	Default
7	**Double Tag Enable** 1 = Double tagging is enabled 0 = Double tagging is disabled	R/W	0b
6:2	**RESERVED**	RO	0x00
1	**Soft Hardware Reset** When set to 1, all register settings, except configuration strap options, are reset to default values.	R/W SC	0b
0	**Start Switch** 1 = Switch function is enabled 0 = Switch function is disabled; no traffic will be passed until this bit is set	R/W	Note 5-3

Note 5-3 The default value of this field is determined by the **LED5_1** configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.1.4.2 Switch MAC Address 0 Register

Address: 0x0302 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [47:40]** This register, along with the Switch MAC Address 1-5 Registers, define the switch's MAC address to be used as the source address in MAC pause control frames, and for self-address filtering.	R/W	0x00

5.1.4.3 Switch MAC Address 1 Register

Address: 0x0303 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [39:32]**	R/W	0x10

5.1.4.4 Switch MAC Address 2 Register

Address: 0x0304 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [31:24]**	R/W	0xA1

5.1.4.5 Switch MAC Address 3 Register

Address: 0x0305 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [23:16]**	R/W	0xFF

5.1.4.6 Switch MAC Address 4 Register

Address: 0x0306 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [15:8]**	R/W	0xFF

5.1.4.7 Switch MAC Address 5 Register

Address: 0x0307 Size: 8 bits

Bits	Description	Type	Default
7:0	**MAC Address [7:0]**	R/W	0xFF

5.1.4.8 Switch Maximum Transmit Unit Register

Address: 0x0308 - 0x0309 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	00b
13:0	**Maximum Frame Length (MTU)** Specifies the maximum transmission unit (MTU), which is the maximum frame payload size. Frames which exceed this maximum are truncated. This value can be set as high as 9000 (= 0x2328) if jumbo frame support is required. Also refer to the Switch MAC Control 1 Register and Port MAC Control 0 Register.	R/W	0x07D0

5.1.4.9 Switch ISP TPID Register

Address: 0x030A - 0x030B Size: 16 bits

Bits	Description	Type	Default
15:0	**ISP Tag TPID** Default tag TPID (EtherType) for untagged incoming frames or the ISP frame tag TPID for the double tagging function.	R/W	0x9100

5.1.4.10 AVB Credit Based Shaper Strategy Register

Address: 0x030E - 0x030F Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	0x0000
1	**Shaping Credit Accounting** 1 = Shaper credit deduction occurs on both data and IPG + preamble 0 = Shaper credit deduction occurs on data only	R/W	1b
0	**Policing Credit Accounting** 1 = Policing credit deduction occurs on both data and IPG + preamble 0 = Policing credit deduction occurs on data only	R/W	1b

5.1.4.11 Switch Lookup Engine Control 0 Register

Address: 0x0310 Size: 8 bits

Bits	Description	Type	Default
7	**802.1Q VLAN Enable** This is the master enable for VLAN forwarding and filtering. Note that the VLAN Table must be set up before VLAN mode is enabled. 1 = VLAN mode enabled 0 = VLAN mode disabled	R/W	0b
6	**Drop Invalid VID** 1 = All received packets with invalid VLAN ID are dropped. 0 = Received packets with invalid VLAN ID are forwarded to the host port. Note that the Unknown VID Forwarding feature (Unknown VLAN ID Control Register), if enabled, takes precedence over this bit.	R/W	1b
5:3	**Age Count** This bit, in combination with the Age Period value (Switch Lookup Engine Control 3 Register), determines the aging time of dynamic entries in the address lookup table. This value is used for the Age Count field whenever a dynamic table entry is updated.	R/W	10_0b
2	**Reserved Multicast Lookup Enable** 1 = Enable Reserved Multicast Table 0 = Disable Reserved Multicast Table	R/W	0b
1:0	**HASH_OPTION** Defines the hashing option for mapping entries to the dynamic lookup table. 00, 11 = Entry is mapped directly using the 10 least significant bits of the destination address. 01 = The CRC hashing function is used. 10 = The XOR hashing function is used. Refer to Section 4.4.2.1, "Address Lookup (ALU) Table," on page 26 for additional information.	R/W	01b

5.1.4.12 Switch Lookup Engine Control 1 Register

Address: 0x0311 Size: 8 bits

Bits	Description	Type	Default
7	**Unicast Learning Disable** 1 = Unicast address learning is disabled 0 = Unicast address learning is enabled	R/W	0b
6	**Self-Address Filtering – Global Enable** The source address of received packets is compared to the MAC address in registers Switch MAC Address 0 Register through Switch MAC Address 5 Register, and the packet is dropped if there is a match. Self-address filtering can be enabled on a port-by-port basis by setting the port enable bit in the Port Control 2 Register in addition to setting this bit. 1 = Enable self-address filtering globally for those ports whose port enable bit (Port Control 2 Register) is set. 0 = Do not filter self-addressed packets on any port.	R/W	0b
5	**Flush Address Lookup Table** The Flush Option bit in the Switch Lookup Engine Control 2 Register determines whether flushing is performed on dynamic entries, static entries, or both. 1 = Trigger a flush of the entire address lookup table. The static address table is not flushed. 0 = Normal operation	R/W SC	0b
4	**Flush MSTP Address Entries (Address Lookup Table)** The Flush Option bit in the Switch Lookup Engine Control 2 Register determines whether flushing is performed on dynamic entries, static entries, or both. 1 = Trigger a flush of the matched MSTP entries 0 = Normal operation	R/W SC	0b
3	**Multicast Source Address Filtering** 1 = Forward packets with a multicast source address 0 = Drop packets with a multicast source address	R/W	1b
2	**Aging Enable** 1 = Enable address table aging 0 = Disable address table aging	R/W	1b
1	**Fast Aging** 1 = Enable fast aging 0 = Disable fast aging	R/W	0b
0	**Link Down Flush** 1 = Link down will cause the entries of any link down port to be flushed 0 = Link down flush is disabled	R/W	0b

5.1.4.13 Switch Lookup Engine Control 2 Register

Address: 0x0312 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	R/W	0b
6	**Double Tag Multicast Trap** 1 = When double tagging mode is enabled, forward all reserved multicast packets to the host port only. 0 = Normal forwarding	R/W	0b
5	**Dynamic Entry Egress VLAN Filtering** Egress VLAN filtering uses the forwarding port map from the VLAN table to restrict the forwarding ports determined from the address lookup. This is the recommended mode of operation when VLAN is enabled. The default value is 0 only for backwards compatibility with previous switches. 1 = Enable. For successful lookup of a dynamic entry in the address table, the forwarding ports are determined from the AND function of the address table port map and the VLAN table port map. 0 = Disable. For successful lookup of a dynamic entry in the address table, the forwarding ports are determined from the address table only.	R/W	0b
4	**Static Entry Egress VLAN Filtering** Egress VLAN filtering uses the forwarding port map from the VLAN table to restrict the forwarding ports determined from the address lookup. This is the recommended mode of operation when VLAN is enabled. The default value is 0 only for backwards compatibility with previous switches. 1 = Enable. For successful lookup of a static entry in the address table, the forwarding ports are determined from the AND function of the address table port map and the VLAN table port map. 0 = Disable. For successful lookup of a static entry in the address table, the forwarding ports are determined from the address table only.	R/W	0b
3:2	**Flush Option** Determines which address lookup table entries may be flushed by either of the flush operations in the Switch Lookup Engine Control 1 Register. 00 = No flush or flush is done 01 = Flush only dynamic table entries 10 = Flush only static table entries 11 = Flush both static and dynamic table entries	R/W	00b
1:0	**MAC Address Priority** 00 = MAC Address (MACA) priority for a packet is determined from the destination address (DA) lookup 01 = MACA priority for a packet is determined from the source address (SA) lookup 10 = MACA priority for a packet is determined from the higher of the DA and SA lookups 11 = MACA priority for a packet is determined from the lower of the DA and SA lookups	R/W	00b

5.1.4.14 Switch Lookup Engine Control 3 Register

Address: 0x0313 Size: 8 bits

Bits	Description	Type	Default
7:0	**Age Period** This value, multiplied by the Age Count value in the entries of the Address Lookup Table, determines the aging time of dynamic entries in that table. The unit is seconds.	R/W	0x4B

5.1.4.15 Address Lookup Table Interrupt Register

Address: 0x0314 Size: 8 bits

This register provides the detailed interrupt status for the Address Lookup Table. These interrupts are enabled in the Address Lookup Table Mask Register. The LUE interrupt status bit in the Global Interrupt Status Register is the OR of the status bits in this register.

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0x00
2	**Learn Fail Interrupt Status** An Address Lookup Table entry was not learned because all entries in the bucket are static	R/WC	0b
1	**Almost Full Interrupt Status** Interrupt indicates that the Address Lookup Table bucket was almost full (2 or 3 valid entries) when a new static entry was written.	R/WC	0b
0	**Write Fail Interrupt Status** Interrupt indicates that the Address Lookup Table bucket is full and a write failed	R/WC	0b

5.1.4.16 Address Lookup Table Mask Register

Address: 0x0315 Size: 8 bits

This register masks the Address Lookup Table interrupts in the Address Lookup Table Interrupt Register.

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0x00
2	**Learn Fail Interrupt Mask** 1 = Interrupt is disabled 0 = Interrupt is enabled	R/W	1b
1	**Almost Full Interrupt Mask** 1 = Interrupt is disabled 0 = Interrupt is enabled	R/W	1b
0	**Write Fail Interrupt Mask** 1 = Interrupt is disabled 0 = Interrupt is enabled	R/W	1b

5.1.4.17 Address Lookup Table Entry Index 0 Register

Address: 0x0316 - 0x0317 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	RO	0x0
11:0 / 9:0	**Almost Full Entry Index [11:0]** When a static entry is successfully written into the Address Lookup Table, but the table bucket is almost full (contains 2 or 3 static entries prior to the write), the entry address is reported here. **Fail Write Index [9:0]** When a static entry write failure occurs in the Address Lookup Table, the bucket address is reported here.	RO	0x000

5.1.4.18 Address Lookup Table Entry Index 1 Register

Address: 0x0318 - 0x0319 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	0000_00
9:0	**Fail Learn Index** When a destination address fails to be learned in the Address Lookup Table because the bucket contains 4 static entries, the bucket address is reported here.	RO	0x000

5.1.4.19 Address Lookup Table Entry Index 2 Register

Address: 0x031A - 0x031B Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	0000_00
9:0	**CPU Access Index** Whenever there is an external read or write to the Address Lookup Table, the bucket address of the access is reported here.	RO	0x000

5.1.4.20 Unknown Unicast Control Register

Address: 0x0320 - 0x0323 Size: 32 bits

The following three registers control forwarding of packets with 1) unknown unicast destination address, 2) unknown multicast destination address, and 3) unknown VLAN ID.

If a received packet falls into more than one of these categories, the precedence is:

1. Unknown VID
2. Unknown Unicast
3. Unknown Multicast

Bits	Description	Type	Default
31	**Unknown Unicast Packet Forward** 1 = Enable forwarding of unknown unicast packets to the ports specified below 0 = Disable unknown unicast packet forwarding	R/W	0b
30:7	**RESERVED**	RO	0x000000
6:0	**Unknown Unicast Forwarding Ports** Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward unknown unicast packets to that port 0 = Do not forward to that port All ones = Forwarded to all ports All zeros = Forwarded to no ports	R/W	000_0000b

5.1.4.21 Unknown Multicast Control Register

Address: 0x0324 - 0x0327 Size: 32 bits

Bits	Description	Type	Default
31	**Unknown Multicast Packet Forward** 1 = Enable forwarding of unknown multicast packets to the ports specified below 0 = Disable unknown multicast packet forwarding	R/W	0b
30:7	**RESERVED**	RO	0x000000
6:0	**Unknown Multicast Forwarding Ports** Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward unknown multicast packets to that port 0 = Do not forward to that port All ones = Forwarded to all ports All zeros = Forwarded to no ports	R/W	000_0000b

5.1.4.22 Unknown VLAN ID Control Register

Address: 0x0328 - 0x032B Size: 32 bits

Bits	Description	Type	Default
31	**Unknown VID Packet Forward** 1 = Enable forwarding of unknown VLAN ID (VID) packets to the ports specified below 0 = Disable unknown VID packet forwarding	R/W	0b
30:7	**RESERVED**	RO	0x000000
6:0	**Unknown VID Forwarding Ports** Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward unknown VID packets to that port 0 = Do not forward to that port All ones = Forwarded to all ports All zeros = Forwarded to no ports	R/W	000_0000b

5.1.4.23 Switch MAC Control 0 Register

Address: 0x0330 Size: 8 bits

Bits	Description	Type	Default
7	**Alternate Back-off Mode** The back-off mode applies to half-duplex only. This bit should be set if the No Excessive Collision Drop bit in the Switch MAC Control 1 Register is enabled. 1 = Enable alternate back-off mode 0 = Disable	R/W	0b
6:4	**RESERVED**	R/W	000b
3	**Frame Length Field Check** This applies only when the EtherType/Length field is <1500. 1 = Discard any packet if the actual packet length does not match the frame length field. 0 = Do not check the packet length.	R/W	0b
2	**RESERVED**	R/W	1b
1	**Flow Control Packet Drop Mode** This bit controls which flow control packets may be forwarded or dropped. To enable forwarding of all flow control packets, refer to bit 0 of the Switch MAC Control 4 Register. Enabling of flow control is managed in the PHY Auto-Negotiation Advertisement Register (for PHY ports) and the XMII Port Control 0 Register (for MAC ports). 1 = The switch will drop received packets with either EtherType = 0x8808 or destination address (DA) = 01-80-C2-00-00-01. 0 = The switch will drop received packets with both EtherType = 0x8808 and DA = 01-80-C2-00-00-01.	R/W	0b
0	**Aggressive Back-off Enable** For use with half-duplex back pressure. This is not an IEEE standard. 1 = Enable aggressive back-off algorithm in half-duplex mode to enhance performance. 0 = Disable	R/W	0b

5.1.4.24 Switch MAC Control 1 Register

Address: 0x0331 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	R/W	1b
6	**Multicast Storm Protection Disable** 1 = Multicast packets are not included in Broadcast Storm Protection 0 = Multicast packets are included in Broadcast Storm Protection	R/W	1b
5	**Back Pressure Mode** 1 = Use carrier sense based back pressure mode 0 = Use collision based back pressure mode. (This is the recommended mode.)	R/W	1b
4	**Flow Control and Back Pressure Fair Mode** 1 = Enable fair mode. If a flow controlled ingress port and a non-flow controlled ingress port forward traffic to the same egress port, packets from the non-flow controlled port may be dropped. 0 = Disable fair mode. In this scenario the flow controlled port will be flow controlled, and the non-flow controlled port will be neither flow controlled nor packets dropped.	R/W	1b
3	**No Excessive Collision Drop** If this bit is set, Alternate Back-odd Mode (bit 7 in the Switch MAC Control 0 Register) should also be set. 1 = The switch will not drop packets when 16 or more collisions occur. 0 = The switch will drop packets when 16 or more collisions occur	R/W	0b
2	**Jumbo Packet Support** The programmable packet payload size limit is specified in register 0x0308 – 0x0309, up to a maximum of 9000 bytes. This bit overrides bit 1 of this register. 1 = Enable support for jumbo packets 0 = Disable	R/W	0b
1	**Legal Maximum Packet Size Check Disable** 1 = Accept packets up to 2000 bytes in size. 0 = Accept only standard size packets, up to 1522 bytes for tagged packets, or 1518 bytes for untagged packets. Larger packets will be dropped.	R/W	0b
0	**Pass Short Packet** 1 = Accept packets between 32 and 64 bytes in size. 0 = Accept only standard size packets, at least 64 bytes. Smaller packets are dropped.	R/W	0b

5.1.4.25 Switch MAC Control 2 Register

Address: 0x0332 Size: 8 bits

Bits	Description	Type	Default
7:4	**RESERVED**	R/W	0x0
3	**Null VID Replacement** Describes the behavior when a packet is received with a null (zero) VID. 1 = Replace a null VID with the Port Default VID as defined in the Port Default Tag 0 Register and Port Default Tag 1 Register 0 = No replacement of null VID	R/W	0b
2:0	**Broadcast Storm Protection Rate bits [10:8]** The remainder of this fields bits are in the Switch MAC Control 3 Register. Multiply this value by 64 to determine how many bytes of packet data are allowed on an input port in a preset period. The period is 5ms for a 1000Mbps port, 50ms for a 100Mbps port, or 500ms for a 10Mbps. The default is 1%.	R/W	000b

5.1.4.26 Switch MAC Control 3 Register

Address: 0x0333 Size: 8 bits

Bits	Description	Type	Default
7:0	**Broadcast Storm Protection Rate bits [7:0]** The remainder of this fields bits are in the Switch MAC Control 2 Register. Multiply this value by 64 to determine how many bytes of packet data are allowed on an input port in a preset period. The period is 5ms for a 1000Mbps port, 50ms for a 100Mbps port, or 500ms for a 10Mbps. The default is 1%.	R/W	0x4A

5.1.4.27 Switch MAC Control 4 Register

Address: 0x0334 Size: 8 bits

Bits	Description	Type	Default
7:1	**RESERVED**	RO	0000_000b
0	**Pass Flow Control Packets** 1 = Switch will forward 802.3x PAUSE flow control frames. 0 = Switch will filter PAUSE frames.	R/W	0b

5.1.4.28 Switch MAC Control 5 Register

Address: 0x0335 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6	**RESERVED**	R/W	0b
5:4	**Ingress Rate Limit Period** 00 = 16ms 01 = 64ms 1x = 256ms	R/W	01b
3	**Queue Based Egress Rate Limit Enable** 1 = Queue-based egress rate limiting 0 = Port-based egress rate limiting	R/W	0b
2:0	**RESERVED**	RO	000b

5.1.4.29 Switch MIB Control Register

Address: 0x0336 Size: 8 bits

MIB counters are provided on a per-port basis. They are read and controlled via the Port N: Port Switch MIB Counters Registers (0xN500 - 0xN5FF).

Bits	Description	Type	Default
7	**Flush MIB Counters** 1 = Flush all MIB counters of enabled ports. Refer to the Port MIB Control and Status Register. 0 = Normal counter operation	R/W SC	0b
6	**Freeze MIB Counters** 1 = Freeze MIB counters of enabled ports. Refer to the Port MIB Control and Status Register. 0 = Normal counter operation	R/W	0b
5:0	**RESERVED**	RO	00_0000b

5.1.4.30 802.1p Priority Mapping 0 Register

Address: 0x0338 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When the tag PCP field is 0x1, use this value for priority**	R/W	001b
3	**RESERVED**	RO	0b
2:0	**When the tag PCP field is 0x0, use this value for priority**	R/W	000b

5.1.4.31 802.1p Priority Mapping 1 Register

Address: 0x0339 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When the tag PCP field is 0x3, use this value for priority**	R/W	011b
3	**RESERVED**	RO	0b
2:0	**When the tag PCP field is 0x2, use this value for priority**	R/W	010b

5.1.4.32 802.1p Priority Mapping 2 Register

Address: 0x033A Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When the tag PCP field is 0x5, use this value for priority**	R/W	101b
3	**RESERVED**	RO	0b
2:0	**When the tag PCP field is 0x4, use this value for priority**	R/W	100b

5.1.4.33 802.1p Priority Mapping 3 Register

Address: 0x033B Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When the tag PCP field is 0x7, use this value for priority**	R/W	111b
3	**RESERVED**	RO	0b
2:0	**When the tag PCP field is 0x6, use this value for priority**	R/W	110b

5.1.4.34 IP DiffServ Priority Enable Register

Address: 0x033E Size: 8 bits

Bits	Description	Type	Default
7:2	**RESERVED**	RO	0000_00b
1	**RESERVED**	R/W	0b
0	**DiffServ Priority Remap Enable** 1 = Use the following registers to remap the DSCP (DiffServ) priority to a 3-bit priority value 0 = Use DSCP bits [5:3] for priority	R/W	0b

5.1.4.35 IP DiffServ Priority Mapping 0 Register

Address: 0x0340 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x01, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x00, use this value for priority**	R/W	000b

5.1.4.36 IP DiffServ Priority Mapping 1 Register

Address: 0x0341 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x03, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x02, use this value for priority**	R/W	000b

5.1.4.37 IP DiffServ Priority Mapping 2 Register

Address: 0x0342 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x05, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x04, use this value for priority**	R/W	000b

5.1.4.38 IP DiffServ Priority Mapping 3 Register

Address: 0x0343 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x07, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x06, use this value for priority**	R/W	000b

5.1.4.39 IP DiffServ Priority Mapping 4 Register

Address: 0x0344 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x09, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x08, use this value for priority**	R/W	000b

5.1.4.40 IP DiffServ Priority Mapping 5 Register

Address: 0x0345 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x0B, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x0A, use this value for priority**	R/W	000b

5.1.4.41 IP DiffServ Priority Mapping 6 Register

Address: 0x0346 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x0D, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x0C, use this value for priority**	R/W	000b

5.1.4.42 IP DiffServ Priority Mapping 7 Register

Address: 0x0347 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x0F, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x0E, use this value for priority**	R/W	000b

5.1.4.43 IP DiffServ Priority Mapping 8 Register

Address: 0x0348 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x11, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x10, use this value for priority**	R/W	000b

5.1.4.44 IP DiffServ Priority Mapping 9 Register

Address: 0x0349 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x13, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x12, use this value for priority**	R/W	000b

5.1.4.45 IP DiffServ Priority Mapping 10 Register

Address: 0x034A Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x15, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x14, use this value for priority**	R/W	000b

5.1.4.46 IP DiffServ Priority Mapping 11 Register

Address: 0x034B Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x17, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x16, use this value for priority**	R/W	000b

5.1.4.47 IP DiffServ Priority Mapping 12 Register

Address: 0x034C Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x19, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x18, use this value for priority**	R/W	000b

5.1.4.48 IP DiffServ Priority Mapping 13 Register

Address: 0x034D Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x1B, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x1A, use this value for priority**	R/W	000b

5.1.4.49 IP DiffServ Priority Mapping 14 Register

Address: 0x034E Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x1D, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x1C, use this value for priority**	R/W	000b

5.1.4.50 IP DiffServ Priority Mapping 15 Register

Address: 0x034F Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x1F, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x1E, use this value for priority**	R/W	000b

5.1.4.51 IP DiffServ Priority Mapping 16 Register

Address: 0x0350 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x21, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x20, use this value for priority**	R/W	000b

5.1.4.52 IP DiffServ Priority Mapping 17 Register

Address: 0x0351 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x23, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x22, use this value for priority**	R/W	000b

5.1.4.53 IP DiffServ Priority Mapping 18 Register

Address: 0x0352 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x25, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x24, use this value for priority**	R/W	000b

5.1.4.54 IP DiffServ Priority Mapping 19 Register

Address: 0x0353 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x27, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x26, use this value for priority**	R/W	000b

5.1.4.55 IP DiffServ Priority Mapping 20 Register

Address: 0x0354 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x29, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x28, use this value for priority**	R/W	000b

5.1.4.56 IP DiffServ Priority Mapping 21 Register

Address: 0x0355 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x2B, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x2A, use this value for priority**	R/W	000b

5.1.4.57 IP DiffServ Priority Mapping 22 Register

Address: 0x0350 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x2D, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x2C, use this value for priority**	R/W	000b

5.1.4.58 IP DiffServ Priority Mapping 23 Register

Address: 0x0357 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x2F, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x2E, use this value for priority**	R/W	000b

5.1.4.59 IP DiffServ Priority Mapping 24 Register

Address: 0x0358 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x31, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x30, use this value for priority**	R/W	000b

5.1.4.60 IP DiffServ Priority Mapping 25 Register

Address: 0x0359 Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x33, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x32, use this value for priority**	R/W	000b

5.1.4.61 IP DiffServ Priority Mapping 26 Register

Address: 0x035A Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x35, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x34, use this value for priority**	R/W	000b

5.1.4.62 IP DiffServ Priority Mapping 27 Register

Address: 0x035B Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x37, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x36, use this value for priority**	R/W	000b

5.1.4.63 IP DiffServ Priority Mapping 28 Register

Address: 0x035C Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x39, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x38, use this value for priority**	R/W	000b

5.1.4.64 IP DiffServ Priority Mapping 29 Register

Address: 0x035D Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x3B, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x3A, use this value for priority**	R/W	000b

5.1.4.65 IP DiffServ Priority Mapping 30 Register

Address: 0x035E Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x3D, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x3C, use this value for priority**	R/W	000b

5.1.4.66 IP DiffServ Priority Mapping 31 Register

Address: 0x035F Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:4	**When IPv4 / IPv6 DSCP field is 0x3F, use this value for priority**	R/W	000b
3	**RESERVED**	RO	0b
2:0	**When IPv4 / IPv6 DSCP field is 0x3E, use this value for priority**	R/W	000b

5.1.4.67 Global Port Mirroring and Snooping Control Register

Address: 0x0370 Size: 8 bits

This register contains global controls for port mirroring and IGMP and MLD snooping. Mirroring also requires additional register settings for the individual ports. Refer to the Port N: Port Switch Ingress Control Registers (0xN800 - 0xN8FF).

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6	**IGMP Snooping Enable (IPv4)** 1 = IGMP snooping is enabled. All IGMP packets will be forwarded to the host port. 0 = IGMP snooping is disabled.	R/W	0b
5:4	**RESERVED**	RO	00b
3	**MLD Snooping Option** 1 = Snooping criteria: IPv6 next header = 43, 44, 50, 51 or 60; or next header = 0 and hop-by-hop next header = 43, 44, 50, 51 or 60. 0 = Snooping criteria: IPv6 next header = 1 or 58; or next header = 0 and hop-by-hop next header = 1 or 58.	R/W	0b
2	**MLD Snooping Enable (IPv6)** 1 = MLD snooping is enabled. All MLD packets will be forwarded to the host port. 0 = MLD snooping is disabled.	R/W	0b
1	**RESERVED**	RO	0b

Bits	Description	Type	Default
0	**Sniff Mode Select** 1 = Sniffing filter is “Rx AND Tx”. Both the source port and destination ports need to match. 0 = Sniffing filter is “Rx OR Tx”. Either the source port of the destination port needs to match. This mode is used to implement Rx-only sniffing.	R/W	0b

5.1.4.68 WRED DiffServ Color Mapping Register

Address: 0x0378 Size: 8 bits

Bits	Description	Type	Default
7:6	**RESERVED**	RO	00b
5:4	**Red** This field specifies the red Differentiated Services Code Point (DSCP) value.	R/W	11b
3:2	**Yellow** This field specifies the yellow DSCP value.	R/W	10b
1:0	**Green** This field specifies the green DSCP value.	R/W	01b

5.1.4.69 PTP Event Message Priority Register

Address: 0x037C Size: 8 bits

Bits	Description	Type	Default
7	**PTP Event Message Priority Override** 0 = PTP event messages are assigned priority based on packet QoS 1 = PTP event messages are forced to the priority assigned to the PTP Event Message Priority field of this register.	R/W	0b
6:4	**RESERVED**	RO	000b
3:0	**PTP Event Message Priority** PTP non-event messages are assigned to this priority on queuing when bit 7 of this register is 1.	R/W	1111b

5.1.4.70 PTP Non-Event Message Priority Register

Address: 0x037D Size: 8 bits

Bits	Description	Type	Default
7	**PTP Non-Event Message Priority Override** 0 = PTP non-event messages are assigned priority based on packet QoS 1 = PTP non-event messages are forced to the priority assigned to the PTP Non-Event Message Priority field of this register.	R/W	0b
6:4	**RESERVED**	RO	000b
3:0	**PTP Non-Event Message Priority** PTP non-event messages are assigned to this priority on queuing when bit 7 of this register is 1.	R/W	1111b

5.1.4.71 Queue Management Control 0 Register

Address: 0x0390 - 0x0393 Size: 32 bits

Bits	Description	Type	Default
31:8	**RESERVED**	RO	0x000000
7:6	**Priority_2Q** When the 2 queue configuration is selected, this determines how to map the 2-bit priority regeneration result from the Port Priority to Queue Mapping Register into 2 queues. 00 = Priorities 0, 1, 2 map to the Low priority queue. Priority 3 maps to the High priority queue. 01 = Not used. 10 = Priorities 0, 1 map to the Low priority queue. Priorities 2, 3 map to the High priority queue. 11 = Priority 0 maps to the Low priority queue. Priorities 1, 2, 3 map to the High priority queue.	R/W	10b
5:2	**RESERVED**	R/W	00_00b
1	**Unicast Port VLAN Membership Discard** This bit applies to the Port VLAN Membership function in registers 0xNA04-07. 1 = All frames are restricted to the forwarding ports as defined in the Port Control 1 Register. 0 = Frames forwarding to a single destination port are not limited to the forwarding ports defined in the Port Control 1 Register. Note that when mirroring is enabled, a single-destination frames will be dropped if it is mirrored to another port.	R/W	1b
0	**RESERVED**	R/W	0b

5.1.5 GLOBAL SWITCH LOOK UP ENGINE (LUE) CONTROL REGISTERS (0x0400 - 0x04FF)

The following registers are used for accessing the VLAN Table, Address Lookup Table, Static Address Table and the Reserved Multicast Address Table. The organizations of these tables, and instructions for accessing them, are provided in Section 5.3, "Tables and MIB Counters (Access)," on page 183.

5.1.5.1 VLAN Table Entry 0 Register

Address: 0x0400 - 0x403 Size: 32 bits

Bits	Description	Type	Default
31	**VALID** This field in the VLAN Table specifies if the table entry is valid. 1 = Table entry is valid 0 = Table entry is invalid	R/W	0b
30:28	**RESERVED**	RO	000b
27	**FORWARD OPTION** This field in the VLAN Table specifies how the forwarding ports are determined. 1 = Forward to the VLAN Table port map (PORT FORWARD field). 0 = Forwarding ports are determined by other variables. It may be the ALU port map, the VLAN port map, the combination of the two, or the Unknown Unicast/Multicast feature.	R/W	0b
26:24	**PRIORITY** This field in the VLAN Table specifies the priority level.	R/W	000b
23:15	**RESERVED**	RO	0000_0000_0b
14:12	**MSTP INDEX** This field in the VLAN Table specifies the Multiple Spanning Tree Protocol index.	R/W	000b
11:7	**RESERVED**	RO	0000_0b
6:0	**FID** This field in the VLAN Table specifies the Filter ID. The FID value is normally combined with the destination address and then hashed to index the address lookup table.	R/W	000_0000b

Note: Refer to Section 5.3.4, "VLAN Table," on page 190 for additional information on VLAN tables.

5.1.5.2 VLAN Table Entry 1 Register

Address: 0x0404 - 0x407 Size: 32 bits

Bits	Description	Type	Default
31:7	**RESERVED**	R/O	0x0000000
6:0	**PORT UNTAG** This field in the VLAN Table specifies the untagging policy for each egress port. Bits [6:0] correspond to ports [7:1]. 1 = Untag packets upon egress at this port 0 = Do not untag upon egress at this port	R/W	0x00

Note: Refer to Section 5.3.4, "VLAN Table," on page 190 for additional information on VLAN tables.

5.1.5.3 VLAN Table Entry 2 Register

Address: 0x0408 - 0x040B Size: 32 bits

Bits	Description	Type	Default
31:7	**RESERVED**	R/O	0x0000000
6:0	**PORT FORWARD** This field specifies the forwarding policy to each port. The policy is applied if the FO bit is set. Bits [6:0] correspond to ports [7:1]. 1 = Forward to this port 0 = Do not forward to this port	R/W	0x00

Note: Refer to Section 5.3.4, "VLAN Table," on page 190 for additional information on VLAN tables.

5.1.5.4 VLAN Table Index Register

Address: 0x040C - 0x040D Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	RO	0x0
11:0	**VLAN Index** This value addresses the VLAN table, in combination with the VLAN table action in the following register.	R/W	0x000

Note: Refer to Section 5.3.4, "VLAN Table," on page 190 for additional information on VLAN tables.

5.1.5.5 VLAN Table Access Control Register

Address: 0x040E Size: 8 bits

Bits	Description	Type	Default
7	**Start VLAN Table Action** 1 = Start the action defined below 0 = Action finished	R/W SC	0b
6:2	**RESERVED**	RO	000_00b
1:0	**Action** Specify the action to be taken for the VLAN table entry addressed in the index register 00 = No operation 01 = Write 10 = Read 11 = Clear all entries to zero	R/W	00b

Note: Refer to Section 5.3.4, "VLAN Table," on page 190 for additional information on VLAN tables.

5.1.5.6 ALU Table Index 0 Register

Address: 0x0410 - 0x0413 Size: 32 bits

The ALU Table Index 0 Register and ALU Table Index 1 Register contain the index values for searching and reading/writing the address lookup table as specified by the action in the ALU Table Access Control Register. For additional information on ALU tables, refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183.

Bits	Description	Type	Default
31	**RESERVED**	R/W	0b
30:23	**RESERVED**	RO	000_0000_0b
22:16	**FID Index [6:0]** This is the FID value used to hash index the table	R/W	000_0000b
15:0	**MAC Index [47:32]** These are the upper 16 bits of the MAC addressed used to hash index the table	R/W	0x0000

5.1.5.7 ALU Table Index 1 Register

Address: 0x0414 - 0x0417 Size: 32 bits

The ALU Table Index 0 Register and ALU Table Index 1 Register contain the index values for searching and reading/writing the address lookup table as specified by the action in the ALU Table Access Control Register. For additional information on ALU tables, refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183.

Bits	Description	Type	Default
31:0	**MAC Index [31:0]** These are the lower 32 bits of the MAC addressed used to hash index the address lookup table. If direct addressing is enabled, then bits [11:0] are used to directly index the address lookup table.	R/W	0x00000000

5.1.5.8 ALU Table Access Control Register

Address: 0x0418 - 0x041B Size: 32 bits

This register provides control and status for searching and reading or writing the ALU Table. The ALU Table Index 0 Register and ALU Table Index 1 Register contain the index values, while the ALU / Static Address Table Entry 1 Register, ALU / Static Address / Reserved Multicast Table Entry 2 Register, ALU / Static Address Table Entry 3 Register, and ALU / Static Address Table Entry 4 Register are used for the entry values. Refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183 for additional information on ALU tables.

Bits	Description	Type	Default
31:30	**RESERVED**	RO	00b
29:16	**VALID_COUNT** Indicates the total number of valid entries in the table after the search finishes	RO	0x0000
15:8	**RESERVED**	RO	0x00
7	**START_FINISH** 1 = Start the action defined below 0 = Action finished	R/W, SC	0b
6	**VALID** For search operation. It is cleared when register 0x042F (ALU / Static Address Table Entry 4 Register) is read. 1 = Indicates that the next valid entry is ready 0 = Next valid entry is not ready	RO	0b
5	**VALID_ENTRY_OR_SEARCH_END** For search operation. It is intended for added convenience when accessing registers by in-band management (IBA) rather than SPI or I^2C. It combines bits 6 and 7. 1 = Indicates either that the next valid entry is ready, or that the search has ended. 0 = Neither next valid entry ready nor search ended.	RO	0b
4:3	**RESERVED**	R/W	00b

Bits	Description	Type	Default
2	**DIRECT** 1 = Access by direct addressing the ALU Table. This method is used only for debugging, if at all. 0 = Hashing function is used to index the table. This is the normal method. Refer to the Switch Lookup Engine Control 0 Register.	R/W	0b
1:0	**ACTION** Specifies the action to be taken for the ALU Table entry access 00 = No operation 01 = Write 10 = Read 11 = Search	R/W	00b

5.1.5.9 Static Address and Reserved Multicast Table Control Register

Address: 0x041C - 0x041F Size: 32 bits

This register provides control and index for reading and writing the Static Address Table and the Reserved Multicast Table. The ALU / Static Address Table Entry 1 Register, ALU / Static Address / Reserved Multicast Table Entry 2 Register, ALU / Static Address Table Entry 3 Register, and ALU / Static Address Table Entry 4 Register are used for the Static Address Table entry values, while only the ALU / Static Address / Reserved Multicast Table Entry 2 Register is used for the Reserved Multicast Table entry value. Refer to Section 5.3.2, "Static Address Table," on page 187 and Section 5.3.3, "Reserved Multicast Address Table," on page 189 for additional information on these tables.

Bits	Description	Type	Default
31:22	**RESERVED**	RO	0x000
21:16	**TABLE_INDEX** Bits [21:16] used to index the Reserved Multicast Table Bits [19:16] used to index the Static Address Table	R/W	00_0000b
15:8	**RESERVED**	RO	0x00
7	**START_FINISH** 1 = Start access 0 = Access is finished	R/W, SC	0b
6:2	**RESERVED**	R/W	000_00b
1	**TABLE_SELECT** Specifies which table is being accessed 1 = Access Reserved Multicast Table 0 = Access Static Address Table	R/W	0b
0	**ACTION** Specifies the action to be taken for the table 1 = Read 0 = Write	R/W	0b

5.1.5.10 ALU / Static Address Table Entry 1 Register

Address: 0x0420 - 0x0423 Size: 32 bits

This register contains the table entry values for read and write operations to the Address Lookup Table and Static Address Table. The field definitions of this register differ dependent on the table type used, as defined in the following sections:

- ALU Table Entry 1 Register on page 186
- Static Address Table Entry 1 Register on page 188

Refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183 and Section 5.3.2, "Static Address Table," on page 187 for additional information.

5.1.5.11 ALU / Static Address / Reserved Multicast Table Entry 2 Register

Address: 0x0424 - 0x0427 Size: 32 bits

The field definitions of this register differ dependent on the table type used, as defined in the following sections:

- ALU Table Entry 2 Register on page 186
- Static Address Table Entry 2 Register on page 188
- Reserved Multicast Address Table Entry 2 Register on page 190

Refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183, Section 5.3.2, "Static Address Table," on page 187, and Section 5.3.3, "Reserved Multicast Address Table," on page 189 for additional information.

5.1.5.12 ALU / Static Address Table Entry 3 Register

Address: 0x0428 - 0x042B Size: 32 bits

The field definitions of this register differ dependent on the table type used, as defined in the following sections:

- ALU Table Entry 3 Register on page 187
- Static Address Table Entry 3 Register on page 189

Refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183 and Section 5.3.2, "Static Address Table," on page 187 for additional information.

5.1.5.13 ALU / Static Address Table Entry 4 Register

Address: 0x042C - 0x042F Size: 32 bits

This register contains the table entry values for read and write operations to the Address Lookup Table and Static Address Table. The field definitions of this register differ dependent on the table type used, as defined in the following sections:

- ALU Table Entry 4 Register on page 187
- Static Address Table Entry 4 Register on page 189

Refer to Section 5.3.1, "Address Lookup (ALU) Table," on page 183 and Section 5.3.2, "Static Address Table," on page 187 for additional information.

5.1.6 GLOBAL SWITCH PTP CONTROL REGISTERS (0x0500 - 0x05FF)

5.1.6.1 Global PTP Clock Control Register

Address: 0x0500 - 0x0501 Size: 16 bits

Bits	Description	Type	Default
15	**Disable Switch Frequency Adjustment** 1 = The switch timers, shapers and policing logic will NOT adjust the frequency based on PTP adjustments. 0 = The switch timers, shapers and policing logic will adjust the frequency based on PTP adjustments.	R/W	0b
14:7	**RESERVED**	RO	000_0000_0b
6	**PTP Clock Step Adjustment** Setting this bit will cause the time value in the Global PTP RTC Clock Nanosecond High Word Register and Global PTP RTC Clock Nanosecond High Word Register to be added to or subtracted from (based on the value of bit 5) the PTP clock.	R/W SC	0b
5	**PTP Step Direction** Direction control for PTP step adjustment mode. 1 = Add the time value 0 = Subtract the time value	R/W	0b
4	**PTP Clock Read** Setting this bit will cause the current PTP clock value to be copied into registers 0x0502 to 0x050B.	R/W SC	0b
3	**PTP Clock Load** Setting this bit will cause the PTP clock to be loaded with the time value in registers 0x0502 to 0x050B.	R/W SC	0b
2	**PTP Clock Continuous Adjustment** When continuous adjustment is enabled, the SUB-NS_RATE value in the Global PTP Clock Sub-Nanosecond Rate High Word Register and Global PTP Clock Sub-Nanosecond Rate Low Word Register is added to or subtracted from (based on the PTP_RATE_DIR bit in the Global PTP Clock Sub-Nanosecond Rate High Word Register) the PTP clock on every 25MHz clock cycle. 1 = Enable continuous adjustment 0 = Disable continuous adjustment	R/W	0b
1	**Enable PTP Clock** 1 = Enable PTP clocking 0 = Disable PTP clocking	R/W	0b
0	**Reset PTP Clock** Setting this bit will reset the PTP clock.	R/W SC	0b

5.1.6.2 Global PTP RTC Clock Phase Register

Address: 0x0502 - 0x0503 Size: 16 bits

Bits	Description	Type	Default
15:3	**RESERVED**	RO	0x0000
2:0	**PTP Real Time Clock 8ns Phase** This register indicates one of the 8n sub-cycle phases of the 40ns period PTP real time clock. 000 = 0ns (real time clock at the first 8ns phase in the 40ns period) 001 = 8ns (real time clock at the second 8ns phase in the 40ns period) 010 = 16ns (real time clock at the third 8ns phase in the 40ns period) 011 = 24ns (real time clock at the fourth 8ns phase in the 40ns period) 100 = 32ns (real time clock at the fifth 8ns phase in the 40ns period) 101 - 111 = not valid	R/W	000b

5.1.6.3 Global PTP RTC Clock Nanosecond High Word Register

Address: 0x0504 - 0x0505 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Real Time Clock Nanosecond [31:16]** This is the high word of the nanosecond value of the PTP real time clock.	R/W	0x0000

5.1.6.4 Global PTP RTC Clock Nanosecond Low Word Register

Address: 0x0506 - 0x0507 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Real Time Clock Nanosecond [15:0]** This is the low word of the nanosecond value of the PTP real time clock.	R/W	0x0000

5.1.6.5 Global PTP RTC Clock Second High Word Register

Address: 0x0508 - 0x0509 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Real Time Clock Second [31:16]** This is the high word of the second value of the PTP real time clock.	R/W	0x0000

5.1.6.6 Global PTP RTC Clock Second Low Word Register

Address: 0x050A - 0x050B Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Real Time Clock Second [15:0]** This is the low word of the second value of the PTP real time clock.	R/W	0x0000

5.1.6.7 Global PTP Clock Sub-Nanosecond Rate High Word Register

Address: 0x050C - 0x050D Size: 16 bits

Bits	Description	Type	Default
15	**PTP Rate Direction** Rate direction control for PTP clock Temporary Adjustment and Continuous Adjustment modes. 1 = The PTP Clock Sub-nanosecond value (this register and Global PTP Clock Sub-Nanosecond Rate Low Word Register) will be added to the PTP time every 25MHz clock cycle. 0 = The PTP Clock Sub-nanosecond value will be subtracted from the PTP time every 25MHz clock cycle.	R/W	0b
14	**PTP Temporary Adjustment Mode** 1 = Enable temporary incrementing or decrementing of the PTP clock by the PTP Clock Sub-nanosecond value (this register and the Global PTP Clock Sub-Nanosecond Rate Low Word Register) every 25MHz clock cycle, for the duration set in the Global PTP Clock Temp Adjustment Duration High Word Register and Global PTP Clock Temp Adjustment Duration Low Word Register. 0 = Stop temporary adjustment of the PTP clock	R/W	0b
13:0	**PTP Real Time Clock Sub-Nanosecond [29:16]** This is the high word of the sub-nanosecond value of the PTP real time clock.	R/W	0x0000

5.1.6.8 Global PTP Clock Sub-Nanosecond Rate Low Word Register

Address: 0x050E - 0x050F Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Real Time Clock Sub-Nanosecond [15:0]** This is the low word of the sub-nanosecond value of the PTP real time clock. It is used for Continuous Adjustment and Temporary Adjustment modes.	R/W	0x0000

5.1.6.9 Global PTP Clock Temp Adjustment Duration High Word Register

Address: 0x0510 - 0x0511 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Temporary Adjustment Duration [31:16]** This sets the duration for the PTP clock temporary rate adjustment, in number of 25MHz clock cycles.	R/W	0x0000

5.1.6.10 Global PTP Clock Temp Adjustment Duration Low Word Register

Address: 0x0512 - 0x0513 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP Temporary Adjustment Duration [15:0]** This sets the duration for the PTP clock temporary rate adjustment, in number of 25MHz clock cycles.	R/W	0x0000

5.1.6.11 Global PTP Message Config 1 Register

Address: 0x0514 - 0x0515 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	0x00
7	**Enable IEEE 802.3AS Mode** 1 = enable 0 = disable	R/W	0b
6	**Enable IEEE 1588 PTP Mode** 1 = enable 0 = disable	R/W	0b
5	**Enable Detection of IEEE 802.3 Ethernet PTP Messages** 1 = enable 0 = disable	R/W	1b
4	**Enable Detection of IPv4/UDP PTP Messages** 1 = enable 0 = disable	R/W	1b
3	**Enable Detection of IPv6/UDP PTP Messages** 1 = enable 0 = disable	R/W	1b
2	**Selection of P2P or E2E** 1 = Peer-to-peer (P2P) transparent clock mode 0 = End-to-end (E2E) transparent clock mode	R/W	0b

Bits	Description	Type	Default
1	**Selection of Master or Slave** 1 = Host port is PTP master ordinary clock 0 = Host port is PTP slave ordinary clock	R/W	0b
0	**Selection of One-step or Two-step Operation** 1 = One-step clock mode 0 = Two-step clock mode	R/W	1b

5.1.6.12 Global PTP Message Config 2 Register

Address: 0x0516 - 0x0517 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	RO	000b
12	**Enable Unicast PTP** 1 = The unicast PTP frames can be recognized. If the packet UDP destination port is either 319 or 320 and the frame MAC/IP address is not the PTP reserved address, then the frame will be considered as a unicast PTP frame and the frame forwarding will be decided by regular lookup table. 0 = Only multicast PTP frames will be recognized.	R/W	1b
11	**Enable Alternate Master** 1 = Alternate master clock is supported. The Sync/Delay_Req frames of the same domain received at non-host ports by active master clock of the same domain will be forwarded to the non-host ports. 0 = Alternate master clock is not supported. The Sync/Delay_Req frames of the same domain received at non-host ports by active master clock of the same domain will be discarded on the host port and will be forwarded to the non-host ports if Sync/Delay_Req is for other domains.	R/W	0b
10	**PTP Messages Priority TX Queue** 1 = All PTP messages are assigned to the highest priority TX queue. 0 = Only the PTP event messages are assigned to the highest priority TX queue.	R/W	0b
9	**Enable Checking of Associated Sync and Follow_up PTP messages** Setting this bit will associate Follow_up message with Sync message when it has the same domain, sequenceID and sourcePortID. The PTP frame will be forwarded to the host port if the ID matches.	R/W	0b
8	**Enable Checking of Associated Delay_Req and Delay Resp PTP Messages** Setting this bit will associate Delay_Resp message with Delay_Req message when it has the same domain, sequenceID and sourcePortID. The PTP frame will be forwarded to the host port if the ID matches.	R/W	0b
7	**Enable Checking of Associated Pdelay_Req and Pdelay_Resp PTP Messages** Setting this bit will associate Pdelay_Resp/Pdelay_Resp_Follow_Up message with Pdelay_Req message when it is with the same domain, sequenceID and sourcePortID. The PTP frame will be forwarded to the host port if ID matches.	R/W	0b
6	**RESERVED**	R/W	0b

Bits	Description	Type	Default
5	**Enable Dropping of Sync/Follow_Up and Delay_Req PTP Messages** Setting this bit will enable the device to automatically drop these Sync/ Follow_up and Delay_Req PTP messages if the Best Master Clock (BMC) is not determined.	R/W	0b
4	**Enable Checking of Domain Field** Setting this bit will enable the device to automatically check the domain field of the PTP message with the PTP_DOMAIN in the Global PTP Domain and Version Register. The PTP message will be forwarded to the host port if the domain field matches. Otherwise it will be dropped.	R/W	0b
3	**RESERVED**	R/W	0b
2	**Enable IPv4/UDP Checksum Calculation for Egress Packets** 1 = The switch will re-calculate and generate a 2-byte checksum value when the frame content changes. 0 = The checksum field is set to zero. If the IPv4/UDP checksum is zero, the checksum will remain zero regardless of this bit setting. For IPv6/UDP, the checksum is always updated.	R/W	1b
1	**RESERVED**	R/W	0b
0	**RESERVED**	R/W	0b

5.1.6.13 Global PTP Domain and Version Register

Address: 0x0518 - 0x0519 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	RO	0x0
11:8	**PTP Version** This is the value of the PTP message version number field. All PTP messages will be captured when the receive message version matches the value in this field. All PTP packets will be dropped if the receive PTP message version does not match the value in this field, except for	R/W	0x2
7:0	**PTP Domain** This is the value of the PTP message domain number field. If domain checking is enabled (Global PTP Message Config 2 Register, bit 4), the timestamp capture will be enabled when the receive PTP message domain number matches the value in this field. If domain checking is not enabled, the domain number field will be ignored.	R/W	0x00

5.1.6.14 Global PTP Unit Index Register

Address: 0x0520 - 0x0523 Size: 32 bits

This register is used to index the timestamp unit and trigger unit for accesses to PTP registers in the address range of 0x052C to 0x05B3. The timestamp and trigger units selected in this register will be the units that are read/written when accessing these registers.

Bits	Description	Type	Default
31:9	**RESERVED**	RO	0x00000
8	**Timestamp Unit Index Pointer (TS_PTR_INDEX)** This bit points to the unit/set registers of the timestamp. 1 = Timestamp Unit 1 0 = Timestamp Unit 0	R/W	0b
7:2	**RESERVED**	RO	000000b
1:0	**Trigger Unit Index Pointer (TRIGGER_PTR_INDEX)** This bit points to the unit/set registers of the trigger. 11 = RESERVED 10 = Trigger Unit 2 01 = Trigger Unit 1 00 = Trigger Unit 0	R/W	00b

5.1.6.15 GPIO Status Monitor 0 Register

Address: 0x0524 - 0x0527 Size: 32 bits

Bits	Description	Type	Default
31:19	**RESERVED**	RO	0x000
18:16	**Event Trigger Output Error (TRIGGER_ERROR)** (Bit 18 = Trigger Unit 2, Bit 17 = Trigger Unit 1, Bit 16 = Trigger Unit 0) 1 = The event trigger time is set earlier than the system time clock when the TRIGGER_NOTIFY bit is set to “1” in the Trigger Output Unit Control 1 Register and will generate an interrupt to the host. This bit can be cleared by resetting the TRIGGER_EN bit to “0” in the Timestamp Control and Status Register. 0 = No event trigger error.	R/W1C	000b
15:3	**RESERVED**	RO	0x000
2:0	**Event Trigger Output Unit Done (TRIGGER_DONE)** (Bit 2 = Trigger Unit 2, Bit 1 = Trigger Unit 1, Bit 0 = Trigger Unit 0) 1 = The event trigger output unit has been generated when the TRIGGER_NOTIFY bit is set to “1” in the Trigger Output Unit Control 1 Register (write “1” to clear this bit) and will generate an interrupt to the host. 0 = Event trigger output unit not done.	R/W1C	000b

5.1.6.16 GPIO Status Monitor 1 Register

Address: 0x0528 - 0x052B Size: 32 bits

This register provides the interrupt status for the trigger output unit and timestamp units used with the GPIO. The GPIO pin Output Trigger and Timestamp Unit interrupt status bit in the Global Interrupt Status Register is the OR of the status bits in this register.

Bits	Description	Type	Default
31:19	**RESERVED**	RO	0x0000
18:16	**Trigger Output Unit Interrupt Status** (Bit 18 = Trigger Unit 2, Bit 17 = Trigger Unit 1, Bit 16 = Trigger Unit 0) These three bits provide the interrupt status for the three Trigger Output Units. These interrupts are enabled by setting the TRIGGER_NOTIFY bit in the Trigger Output Unit Control 1 Register. This is done separately for each TOU. Refer to the GPIO Status Monitor 0 Register for the Trigger Output Unit status details. 1 = Interrupt detected 0 = No interrupt	R/WC	000b
15:2	**RESERVED**	RO	0x0000
1:0	**Timestamp Unit Interrupt Status (GPIO input timestamp only)** (Bit 1 = Timestamp Unit 1, Bit 0 = Timestamp Unit 0) These two bits provide the interrupt status for the two Timestamp Output Units for the GPIO. These interrupts are enabled by the Timestamp Unit Interrupt Enable bit in the Timestamp Control and Status Register. This is done separately for each TSU. Refer to the registers beginning at the Timestamp Status and Control Register for Timestamp interrupt details. For the interrupt status for the port-based timestamping of PTP egress frames, refer to the Port Interrupt Status Register and Port PTP Timestamp Interrupt Status Register. 1 = Interrupt detected 0 = No interrupt	R/WC	00b

5.1.6.17 Timestamp Control and Status Register

Address: 0x052C - 0x052F Size: 32 bits

Portions of this register are indexed by the Trigger Unit Index Pointer (bits [1:0]) and Timestamp Unit Index Pointer (bit 8) values in the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:9	**RESERVED**	RO	0x000000
8	**GPIO Output Source Select (GPIO_OUT_SEL)** 1 = The output is a combinatorial result 0 = The output is from flopped output	R/W	0b
7	**GPIO Inputs Monitor (GPIO_IN)** This field reflects the current value seen on the GPIO input.	R	-
6	**GPIO Output Enable (GPIO_OEN)** 1 = Enables the GPIO pin as a trigger input 0 = Enables the GPIO pin as a timestamp input	R/W	0b
5	**Timestamp Unit Interrupt Enable (TS_INT_ENB)** The timestamp unit interrupt status bit is found in the GPIO Status Monitor 1 Register. 0 = Interrupt disabled 1 = Interrupt enabled **Note:** This field is indexed by the Timestamp Unit Index Pointer (bit 8) value in the Global PTP Unit Index Register.	R/W	0b
4	**Event Trigger Output Unit Active (TRIGGER_ACTIVE)** 1 = The event trigger output unit is enabled and active without error 0 = The event trigger output unit is finished and inactive **Note:** This field is indexed by the Trigger Unit Index Pointer (bits 1:0) value in the Global PTP Unit Index Register.	R	0b
3	**Event Trigger Output Unit Enable (TRIGGER_EN)** 1 = Enables the selected event trigger output unit. Self-clearing when trigger output is generated. In cascade mode, only enable the head of the trigger unit. 0 = The event trigger out unit is disabled **Note:** This field is indexed by the Trigger Unit Index Pointer (bits 1:0) value in the Global PTP Unit Index Register.	R/W	0b
2	**Event Trigger Output Unit Software Reset (TRIGGER_SW_RESET)** 1 = Resets the trigger output unit to the inactive state and default settings. This reset can be used to stop the cascade mode in continuous operation and prepare this trigger unit for the next operation. 0 = Trigger output unit under normal operation **Note:** This field is indexed by the Trigger Unit Index Pointer (bits 1:0) value in the Global PTP Unit Index Register.	R/W	0b
1	**Event Timestamp Input Unit Enable (TS_ENB)** 1 = Enables the selected event timestamp input unit. Writing “1” to this bit will clear the TS_EVENT_DET_CNT of the associated unit. 0 = Disables the selected event timestamp input unit. Writing “0” to this bit will clear the TS_RDY and TS_DET_CNT_OVFL. **Note:** This field is indexed by the Timestamp Unit Index Pointer (bit 8) value in the Global PTP Unit Index Register.	R/W	0b

Bits	Description	Type	Default
0	**Event Timestamp Input Unit Software Reset (TS_SW_RESET)** 1 = Resets the timestamp unit to the inactive state and default settings 0 = Timestamp input unit under normal operation **Note:** This field is indexed by the Timestamp Unit Index Pointer (bit 8) value in the Global PTP Unit Index Register.	R/W	0b

5.1.6.18 Trigger Output Unit Target Time Nanosecond Register

Address: 0x0530 - 0x0533 Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:30	**RESERVED**	RO	000b
29:0	**Trigger Target Time (ns) (TRIGGER_TARGET_TIME_NS)** This field contains the PTP event trigger output target time in nanoseconds for the trigger unit indexed in the Global PTP Unit Index Register.	R/W	0x00000000

5.1.6.19 Trigger Output Unit Target Time Second Register

Address: 0x0534 - 0x0537 Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Trigger Target Time (s) (TRIGGER_TARGET_TIME_S)** This field contains the PTP event trigger output target time in seconds for the trigger unit indexed in the Global PTP Unit Index Register.	R/W	0x00000000

5.1.6.20 Trigger Output Unit Control 1 Register

Address: 0x0538 - 0x053B Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**Enable Event Trigger Output Unit in Cascade Mode (CASCADE_MODE_ENB)** 1 = Enables the event trigger output unit in cascade mode 0 = Disables the event trigger output unit in cascade mode	R/W	0b
30	**Cascade Mode Event Trigger Output Unit Tail Unit Indicator (CASCADE_MODE_TAIL)** 1 = This event trigger output unit is the last unit of the chain in cascade mode 0 = This event trigger output unit is not the last unit of the chain in cascade mode. Note: when this bit it cleared to “0” for all units in cascade mode, the iteration count is ignored and becomes an infinite number. To stop the infinite loop, set the respective TRIG_SW_RESET bit in the Timestamp Control and Status Register.	R/W	0b
29:28	**RESERVED**	RO	00b
27:26	**Cascade Mode Upstream Trigger Done Unit Select** This field selects one of the 3 upstream trigger done input units in cascade mode. For example, if units 1, 2, and 3 (tail unit) are set up in cascade mode, then Unit 1 is set to 0x3, Unit 2 is set to 0x1, and Unit 3 is set to 0x2.	R/W	00b
25	**Trigger Now (TRIGGER_NOW)** 1 = Immediately trigger even output if trigger target time is less than the system clock time 0 = Wait for trigger target time to trigger event output	R/W	0b
24	**Trigger Notify (TRIGGER_NOTIFY)** 1 = Enables reporting both TRIG_DONE and TRIG_ERR status as well as interrupt to host if interrupt enable bit is set. 0 = Disables reporting of both TRIG_DONE and TRIG_ERR status.	R/W	0b
23	**Trigger Edge (TRIGGER_EDGE)** 1 = Trigger output on negative edge of clock 0 = Trigger output on positive edge of clock	R/W	0b

Bits	Description	Type	Default
22:20	**Trigger Event Output Signal Pattern (TRIGGER_PATTERN)** To select a trigger event output when TRIG_EN=1 and the trigger target time has reached the system time: **000** = Generates negative edge (from default “H” -> “L” and stays “L”) **001** = Generates positive edge (from default “L” -> “H” and stays “H”) **010** = Generates negative pulse (from default “H” -> “L” pulse -> “H” and stays “H”). The pulse width is defined in the Trigger Output Unit Control 2 Register. **011** = Generates positive pulse (from default “L” -> “H” pulse -> “L” and stays “L”). The pulse width is defined in the Trigger Output Unit Control 2 Register. **100** = Generates negative periodic signal. The “L” pulse width is defined in the Trigger Output Unit Control 2 Register, the cycle width is defined in the Trigger Output Unit Control 3 Register and Trigger Output Unit Control 4 Register, and the number of cycles is defined in the Trigger Output Unit Control 5 Register (it is an infinite number if the number of cycles is zero). **101** = Generates positive periodic signal. The “H” pulse width is defined in the Trigger Output Unit Control 2 Register, the cycle width is defined in the Trigger Output Unit Control 3 Register and Trigger Output Unit Control 4 Register, and the number of cycles is defined in the Trigger Output Unit Control 5 Register (it is an infinite number if the number of cycles is zero). **110** = Generates output signal from the 16-bit pattern in the Trigger Output Unit Control 3 Register, which is shifted MSB fist and looped. Each bit width is defined in the Trigger Output Unit Control 3 Register and Trigger Output Unit Control 4 Register and the total number of bits to shift out is defined in the Trigger Output Unit Control 5 Register (it is infinite if this register value is zero). **111** = RESERVED. **Note:** The maximum output clock frequency is up to 12.5MHz.	R/W	000b
19:16	**RESERVED**	RO	000b
15:0	**Trigger Output Iteration Count (TRIGGER_PATTERN_ITERATION)** Defines the iteration count number to output the 16-bit trigger pattern defined in the Trigger Output Unit Control 3 Register in cascade mode at tail unit. For example, 0x0000 is 1 count and 0x000F is 16 counts. It is infinite if there is no tail unit in cascade mode.	R/W	0x0000

5.1.6.21 Trigger Output Unit Control 2 Register

Address: 0x053C - 0x053F Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Trigger Output Cycle Width or Bit Width (TRIGGER_CYCLE_WIDTH)** Defines the cycle width for generating periodic signals. Each unit value equals 1ns. For example, the cycle width is 80ns if this register value is 80 (0x50).	R/W	0x00000000

5.1.6.22 Trigger Output Unit Control 3 Register

Address: 0x0540 - 0x0543 Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:16	**Trigger Output Cycle or Bit Count (TRIGGER_CYCLE)** Defines the number of output cycles for generating periodic signals. It is infinite if this field is zero.	R/W	0x0000
15:0	**Trigger Output Bit Pattern (TRIGGER_BIT_PATTERN)** Defines the output bit pattern for generating output signals.	R/W	0x0000

5.1.6.23 Trigger Output Unit Control 4 Register

Address: 0x0544 - 0x0547 Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Trigger Output Iteration Cycle Time in Cascade Mode (CASCADE_INTERATION_CYCLE_TIME)** Defines the iteration cycle time to go through all the trigger output units in cascade mode. This time will be added to the current trigger target time for the next trigger time. A unit value equals 1ns. For example, the cycle is 800ns if this field value is 800 (0x320).	R/W	0x00000000

5.1.6.24 Trigger Output Unit Control 5 Register

Address: 0x0548 - 0x054B Size: 32 bits

This register is indexed by the Trigger Unit Index Pointer value in bits [1:0] of the Global PTP Unit Index Register.

This register contains the PTP event trigger output PPS signal pulse width for unit 2 and path delay compensation for unit 1.

Bits	Description	Type	Default
31:24	**RESERVED**	RO	-
23:16	**PPS Pulse Width for Event Trigger (PPS_PULSE_WIDTH)** This field is the upper third byte (23:16) in conjunction with the trigger output pulse width to make this to make this register value for PPS pulse width up to 124ms.	R/W	0x00
15:0	**Trigger Output Pulse Width (TRIGGER_PULSE_WIDTH)** Defines the width for generating a pulse or periodic signal. Each unit value equals 8ns. For example, the pulse width is 80ns if this register value is 10 (0xA).	R/W	0x0000

5.1.6.25 Timestamp Status and Control Register

Address: 0x0550 - 0x0553 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:21	**RESERVED**	RO	0x00
20:17	**Number of Detected Event Count for Timestamp Input Unit (TS_EVENT_DET_CNT)** Reports the number of detected events (either rising or falling edge) count. In single mode, it can detect up to 15 events at any single unit. The pulse or edges can be detected up to 25MHz. The pulse width can be measured by the difference between consecutive timestamps in the same unit.	RO	0000b
16	**Number of Detected Event Count Overflow for Timestamp Input Unit (TS_DET_EVENT_CNT_OVERFLOW)** 1 = The detected events (either rising or falling edge) count has overflowed. In cascade mode, only the tail unit will set this bit when overflow occurs. The TS_EVENT_DET_CNT field will remain at 15 when overflow has occurred. 0 = The number of events (either rising or falling edge) count has not overflowed.	RO	0b
15:8	**RESERVED**	RO	00000000b
7	**Enable Rising Edge Detection (TS_RISING_EDGE_ENB)** 1 = Enable rising edge detection 0 = Disable rising edge detection	R/W	0b
6	**Enable Falling Edge Detection (TS_FALLING_EDGE_ENB)** 1 = Enable falling edge detection 0 = Disable falling edge detection	R/W	0b
5	**Tail Unit Indicator for Timestamp Input Unit Event in Cascade Mode (TS_CASCADE_MODE_TAIL)** 1 = This event timestamp input unit is the last unit of the chain in cascade mode. 0 = This event timestamp input unit is not the last unit of the chain in cascade mode.	R/W	0b
4:2	**RESERVED**	RO	00b
1	**Select Upstream Timestamp Done Unit in Cascade Mode (TS_CASCADE_MODE_ENB)** This bit selects the timestamps done input unit in cascade mode. 1 = Timestamp Unit 1 0 = Timestamp Unit 0 In the head unit, this should be set to “0” so that no upstream timestamp unit will be input to the head unit.	R/W	0b
0	**Enable This Event Timestamp Input Unit in Cascade Mode (TS_CASCADE_MODE_ENB)** 1 = Enables this event timestamp input unit in cascade mode. 0 = Disables this event timestamp input unit in cascade mode.	R/W	0b

5.1.6.26 Timestamp 1st Sample Time Nanoseconds Register

Address: 0x0554 - 0x0557 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 1st Sample Edge Indication (TS_SAMPLE_EDGE_1ST)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 1st Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_1ST)** This field is the low-word of the first sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.27 Timestamp 1st Sample Time Seconds Register

Address: 0x0558 - 0x055B Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 1st Sample Time in Seconds (TS_SAMPLE_TIME_S_1ST)** This field is the first sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.28 Timestamp 1st Sample Time Phase Register

Address: 0x055C - 0x055F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 1st Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_1ST)** This field indicates one of the 8ns cycles for the first sample time of the time-stamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.29 Timestamp 2nd Sample Time Nanoseconds Register

Address: 0x0560 - 0x0563 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 2nd Sample Edge Indication (TS_SAMPLE_EDGE_2ND)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 2nd Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_2ND)** This field is the low-word of the second sample time for the timestamp in nanoseconds.	RO	0x00000000

5.1.6.30 Timestamp 2nd Sample Time Seconds Register

Address: 0x0564 - 0x0567 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 2nd Sample Time in Seconds (TS_SAMPLE_TIME_S_2ND)** This field is the second sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.31 Timestamp 2nd Sample Time Phase Register

Address: 0x0568 - 0x056F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 2nd Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_2ND)** This field indicates one of the 8ns cycles for the second sample time of the timestamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.32 Timestamp 3rd Sample Time Nanoseconds Register

Address: 0x056C - 0x056F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 3rd Sample Edge Indication (TS_SAMPLE_EDGE_3RD)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 3rd Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_3RD)** This field is the low-word of the third sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.33 Timestamp 3rd Sample Time Seconds Register

Address: 0x0570 - 0x0573 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 3rd Sample Time in Seconds (TS_SAMPLE_TIME_S_3RD)** This field is the third sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.34 Timestamp 3rd Sample Time Phase Register

Address: 0x0574 - 0x0577 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 3rd Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_3RD)** This field indicates one of the 8ns cycles for the third sample time of the time-stamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.35 Timestamp 4th Sample Time Nanoseconds Register

Address: 0x0578 - 0x057B Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 4th Sample Edge Indication (TS_SAMPLE_EDGE_4TH)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 4th Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_4TH)** This field is the low-word of the fourth sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.36 Timestamp 4th Sample Time Seconds Register

Address: 0x057C - 0x057F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 4th Sample Time in Seconds (TS_SAMPLE_TIME_S_4TH)** This field is the fourth sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.37 Timestamp 4th Sample Time Phase Register

Address: 0x0580 - 0x0583 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 4th Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_4TH)** This field indicates one of the 8ns cycles for the fourth sample time of the timestamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.38 Timestamp 5th Sample Time Nanoseconds Register

Address: 0x0584 - 0x0587 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 5th Sample Edge Indication (TS_SAMPLE_EDGE_5TH)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 5th Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_5TH)** This field is the low-word of the fifth sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.39 Timestamp 5th Sample Time Seconds Register

Address: 0x0588 - 0x058B Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 5th Sample Time in Seconds (TS_SAMPLE_TIME_S_5TH)** This field is the fifth sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.40 Timestamp 5th Sample Time Phase Register

Address: 0x058C - 0x058F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 5th Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_5TH)** This field indicates one of the 8ns cycles for the fifth sample time of the time-stamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.41 Timestamp 6th Sample Time Nanoseconds Register

Address: 0x0590 - 0x0593 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 6th Sample Edge Indication (TS_SAMPLE_EDGE_6TH)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 6th Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_6TH)** This field is the low-word of the sixth sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.42 Timestamp 6th Sample Time Seconds Register

Address: 0x0594 - 0x0597 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 6th Sample Time in Seconds (TS_SAMPLE_TIME_S_6TH)** This field is the sixth sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.43 Timestamp 6th Sample Time Phase Register

Address: 0x0598 - 0x059B Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 6th Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_6TH)** This field indicates one of the 8ns cycles for the sixth sample time of the time-stamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.44 Timestamp 7th Sample Time Nanoseconds Register

Address: 0x059C - 0x059F Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 7th Sample Edge Indication (TS_SAMPLE_EDGE_7TH)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 7th Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_7TH)** This field is the low-word of the seventh sample time for the timestamp in nanoseconds.	RO	0x00000000

5.1.6.45 Timestamp 7th Sample Time Seconds Register

Address: 0x05A0 - 0x05A3 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 7th Sample Time in Seconds (TS_SAMPLE_TIME_S_7TH)** This field is the seventh sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.46 Timestamp 7th Sample Time Phase Register

Address: 0x05A4 - 0x05A7 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 7th Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_7TH)** This field indicates one of the 8ns cycles for the seventh sample time of the timestamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.1.6.47 Timestamp 8th Sample Time Nanoseconds Register

Address: 0x05A8 - 0x05AB Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31	**RESERVED**	RO	0b
30	**Event Timestamp Input of the 8th Sample Edge Indication (TS_SAMPLE_EDGE_8TH)** 1 = Indicates the event timestamp input is a rising edge signal 0 = Indicates the event timestamp input is a falling edge signal	RO	0b
29:0	**Event Timestamp Input of the 8th Sample Time in Nanoseconds (TS_SAMPLE_TIME_NS_8TH)** This field is the low-word of the eighth sample time for the timestamp in nano-seconds.	RO	0x00000000

5.1.6.48 Timestamp 8th Sample Time Seconds Register

Address: 0x05AC - 0x05AF Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:0	**Event Timestamp Input of the 8th Sample Time in Seconds (TS_SAMPLE_TIME_S_8TH)** This field is the eighth sample time for the timestamp in seconds.	RO	0x00000000

5.1.6.49 Timestamp 8th Sample Time Phase Register

Address: 0x05B0 - 0x05B3 Size: 32 bits

This register is indexed by the Timestamp Unit Index Pointer value in bit 8 of the Global PTP Unit Index Register.

Bits	Description	Type	Default
31:3	**RESERVED**	RO	0x0000000
2:0	**Event Timestamp Input of the 8th Sample Time in Sub 8ns (TS_SAMPLE_TIME_SUB_8NS_8TH)** This field indicates one of the 8ns cycles for the eighth sample time of the timestamp. 000 = 0ns (sample time at the first 8ns cycle in 25MHz/40ns) 001 = 8ns (sample time at the second 8ns cycle in 25MHz/40ns) 101 = 16ns (sample time at the third 8ns cycle in 25MHz/40ns) 011 = 24ns (sample time at the fourth 8ns cycle in 25MHz/40ns) 100 = 32ns (sample time at the fifth 8ns cycle in 25MHz/40ns) 101-111 = RESERVED	RO	000b

5.2 Port Registers

This section details the device's port registers. All settings are on a per-port basis. Address field "N" specifies the port number. Valid values for "N" are 1 to 7 for some registers, 6 to 7 for MAC port specific registers, and 0 to 5 for PHY specific registers.

For an overview of the device's entire register map, refer to Section 5.0, "Device Registers". For details on the device's global registers, refer to Section 5.1, "Global Registers".

5.2.1 PORT N: PORT OPERATION CONTROL REGISTERS (0xN000 - 0xN0FF)

5.2.1.1 Port Default Tag 0 Register

Address: 0xN000 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Port Default 802.1Q Tag [15:8]** Bits [7:5]: Priority Code Point (PCP) Bit [4]: Drop Eligible Indicator (DEI) Bits [3:0]: VLAN Identifier (VID) [11:8]	R/W	0x00

5.2.1.2 Port Default Tag 1 Register

Address: 0xN001 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Port Default 802.1Q tag [7:0]** VLAN Identifier (VID) [7:0]	R/W	0x01

5.2.1.3 Port PME_WoL Event Register

Address: 0xN013 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_0b
2	**Magic Packet Detect** To be detected, the destination address of the Magic Packet must match the Global Switch MAC Address in the Switch MAC Address 0 Register through Switch MAC Address 5 Register. 1 = Magic Packet is detected at this port 0 = Not detected	RO/WC	0b

Bits	Description	Type	Default
1	**Link Up Detect** Applicable only to ports with integrated PHY. 1 = Link up is detected at this port 0 = Not detected	RO/WC	0b
0	**Energy Detect** Applicable only to ports with integrated PHY. 1 = Cable energy is detected at this port 0 = Not detected	RO/WC	0b

5.2.1.4 Port PME_WoL Enable Register

Address: 0xN017 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_0b
2	**Magic Packet Detect Enable** To be detected, the destination address of the Magic Packet must match the Global Switch MAC Address in the Switch MAC Address 0 Register through Switch MAC Address 5 Register. 1 = The PME pin will be asserted when a Magic Packet is detected at this port 0 = The PME pin will not be asserted by Magic Packet detection at this port	RO/WC	0b
1	**Link Up Detect Enable** Applicable only to ports with integrated PHY. 1 = The PME pin will be asserted when link up is detected at this port 0 = The PME pin will not be asserted by link up detection at this port	RO/WC	0b
0	**Energy Detect Enable** Applicable only to ports with integrated PHY. 1 = The PME pin will be asserted when cable energy is detected at this port 0 = The PME pin will not be asserted by cable energy detection at this port	RO/WC	0b

5.2.1.5 Port Interrupt Status Register

Address: 0xN01B Size: 8 bits
Port N: 1-7

These registers provide interrupt status for the individual ports. these interrupts are enabled in the Port Interrupt Mask Register. For non-port specific interrupt status, refer to the Global Interrupt Status Register.

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_00b
2	**PTP Interrupt Status** Applies only to PHY ports, not MAC port(s). Refer to the Port PTP Timestamp Interrupt Status Register for individual PTP interrupts. 0 = No interrupt 1 = Interrupt detected	RO	0b
1	**PHY Interrupt Status** Applies only to PHY ports, not MAC port(s). Refer to the Port Interrupt Control / Status Register for individual PHY interrupts. 0 = No interrupt 1 = Interrupt detected	RO	0b
0	**ACL Interrupt Status** ACL interrupts can be generated by configuring an entry in the ACL Table for counter mode. All ports have an ACL Table. To clear this bit, toggle the ACL Interrupt Mask bit in the Port Interrupt Mask Register. 0 = No interrupt 1 = Interrupt detected	RO	0b

5.2.1.6 Port Interrupt Mask Register

Address: 0xN01F Size: 8 bits
Port N: 1-7

This register enables the interrupts in the Port Interrupt Status Register.

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_00b
2	**PTP Interrupt Enable** Applies only to PHY ports. Refer to the Port PTP Timestamp Interrupt Enable Register for individual PTP interrupt enables. 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b
1	**PHY Interrupt Enable** Applies only to PHY ports. 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b

Bits	Description	Type	Default
0	**ACL Interrupt Enable** Applies to all ports. 0 = Interrupt enabled 1 = Interrupt disabled	R/W	0b

5.2.1.7 Port Operation Control 0 Register

Address: 0xN020 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**Local Loopback** Data going from the internal switch fabric to an egress port is looped back at that egress port and returned to the internal switch fabric. 1 = Local loopback 0 = Normal operation	R/W	0b
6	**Remote Loopback** Data received at the external pins of a port is looped back and sent out the same port, without passing through the internal switch fabric. For PHY ports, data is received on the RX+/- pins and transmitted out the TX+/- pins. For xMII ports, data is received on the TXD pins and transmitted on the RXD pins. 1 = Remote loopback 0 = Normal operation	R/W	0b
5:3	**RESERVED**	RO	000b
2	**Tail Tag Enable** When tail tagging is enabled for a port, it designates that port to be the “host” or “CPU” port. Do not enable tail tagging for more than one port. See the tail tagging description for details. 1 = Enable tail tagging on this port 0 = Disable tail tagging for this port	R/W	0b
1:0	**Egress Queue Split Enable** 11 = Reserved 10 = Four egress queues. Packets are assigned to a queue based on priority. 01 = Two egress queues. Packets are assigned to a queue based on priority. 00 = Single egress queue. There is no priority differentiation.	R/W	00b

5.2.1.8 Port Status Register

Address: 0xN030 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:5	**RESERVED**	RO	000
4:3	**Port Speed Status** For non-PHY ports, these bits duplicate the speed setting in the XMII Port Control 1 Register bit 6 and XMII Port Control 0 Register bit 4. For PHY ports, these bits indicate the actual link speed, which is also available in the PHY Control Register. 00 = 10 Mb/s 01 = 100 Mb/s 10 = 1000 Mb/s	RO	-
2	**Port Duplex Status** For non-PHY ports, this bit duplicates the duplex setting in the XMII Port Control 0 Register bit 6. For PHY ports, this bit indicates the actual link duplex, which is also available in the PHY Control Register. 1 = Full duplex 0 = Half duplex	RO	1 or -
1	**Transmit Flow Control Enabled Status** For non-PHY ports, this bit duplicates the Tx FC enable bit 5 in the XMII Port Control 0 Register. For PHY ports, this bit is set only when FC is enabled (PHY Auto-Negotiation Advertisement Register, bits 11:10), link is up and FC is established via auto-negotiation. 1 = TX flow control is enabled 0 = Disabled	RO	-
0	**Receive Flow Control Enabled Status** For non-PHY ports, this bit duplicates the Rx FC enable bit 3 in the XMII Port Control 0 Register. For PHY ports, this bit is set only when FC is enabled (PHY Auto-Negotiation Advertisement Register, bits 11:10), link is up and FC is established via auto-negotiation. 1 = RX flow control is enabled 0 = Disabled	RO	-

5.2.2 PORT N: PORT ETHERNET PHY REGISTERS (0xN100 - 0xN1FF)

The registers in this section are for PHY ports only. Refer to the IEEE802.3 clause 22.3.4 for additional details.

5.2.2.1 PHY Basic Control Register

Address: 0xN100 - 0xN101 Size: 16 bits
Port N: 1-5

PHY register 0x00.

Bits	Description	Type	Default
15	**PHY Software Reset** Set this bit to reset this PHY. Registers are not reset. This bit is self-clearing.	R/W SC	0b
14	**Local Loopback Mode** Data going from the internal switch fabric to an egress port is looped back at that egress port and returned to the internal switch fabric. 1 = Local Loopback mode 0 = Normal operation	R/W	0b
13	**Speed Select (LSB)** This bit is ignored if auto-negotiation is enabled (bit 12 in this register). 1 = 100 Mb/s 0 = 10 Mb/s	R/W	Note 5-4
12	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled 0 = Auto-negotiation is disabled The initial value of this bit is determined by a strapping option, but it may be overwritten.	R/W	Note 5-4
11	**Power Down** 1 = Power-down mode 0 = Normal operation When this bit is set to ‘1’, the link-down status might not get updated in the PHY status register. Software should note link is down and should not rely on the PHY status register link status. After this bit is changed from ‘1’ to ‘0’, an internal reset is performed. Wait a minimum of 1ms before read/write access to this PHY’s registers.	R/W	0b
10	**Isolate** 1 = Logical isolation of the PHY from the switch core 0 = Normal operation	R/W	0b
9	**Re-start Auto-Negotiation** Set this bit to re-start auto-negotiation. This bit is self-clearing.	R/W, SC	0b
8	**Duplex Mode** This bit is ignored if auto-negotiation is enabled (bit 12 in this register). 1 = Full duplex 0 = Half duplex	R/W	1b
7	**Collision Test** 1 = Enable COL test 0 = Disable COL test	R/W	0b

Bits	Description	Type	Default
6:0	**RESERVED**	RO	0x00

Note 5-4 The default value of this field is determined by the associated configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.2.2.2 PHY Basic Status Register

Address: 0xN102 - 0xN103 Size: 16 bits
Port N: 1-5

PHY register 0x01.

Bits	Description	Type	Default
15	**100BASE-T4** 0 = PHY is not 100BASE-T4 capable	RO	0b
14	**100BASE-TX Full Duplex** 1 = PHY is 100BASE-TX full-duplex capable	RO	1b
13	**100BASE-TX Half Duplex** 1 = PHY is 100BASE-TX half-duplex capable	RO	1b
12	**10 Mb/s Full Duplex** 1 = PHY is 10 Mb/s full-duplex capable	RO	1b
11	**10 Mb/s Half Duplex** 1 = PHY is 10 Mb/s half-duplex capable	RO	1b
10:9	**RESERVED**	RO	00b
8	**Extended Status** 1 = Extended status information available. **Note:** Since the device PHYs only support 10/100Mbps operation, extended status information is not available.	RO	0b
7	**RESERVED**	RO	0b
6	**MF Preamble Suppression** 1 = PHY will accept management frames with preamble suppressed	RO	1b
5	**Auto-negotiation Complete** 1 = Auto-negotiation process is complete 0 = Auto-negotiation process is not complete	RO	-
4	**Remote (Far End) Fault** 1 = Remote fault condition detected 0 = No remote fault detected	RO LH	-
3	**Auto-Negotiation Ability** 1 = PHY is able to perform auto-negotiation	RO	1b
2	**Link Status** 1 = Link is up 0 = Link is down	RO LL	-
1	**Jabber Detect** 1 = Jabber condition detected 0 = No jabber condition detected	RO LH	-

Bits	Description	Type	Default
0	**Extended Capability** 1 = Supports extended capabilities register 0 = Basic register set capabilities only	RO	1b

5.2.2.3 PHY ID High Register

Address: 0xN104 - 0xN105 Size: 16 bits
Port N: 1-5

PHY register 0x02.

Bits	Description	Type	Default
15:0	**PHY Identifier High Word**	RO	0x0022

5.2.2.4 PHY ID Low Register

Address: 0xN106 - 0xN107 Size: 16 bits
Port N: 1-5

PHY register 0x03.

Bits	Description	Type	Default
15:0	**PHY Identifier Low Word**	RO	0x1631

5.2.2.5 PHY Auto-Negotiation Advertisement Register

Address: 0xN108 - 0xN109 Size: 16 bits
Port N: 1-5

PHY register 0x04.

Bits	Description	Type	Default
15	**Next Page** 1 = Next page capable 0 = No next page capability	R/W	0b
14	**RESERVED**	RO	0b
13	**Remote Fault** 1 = Remote fault capable 0 = No remote fault capability	R/W	0b
12	**RESERVED**	RO	0b
11:10	**Pause (Flow Control) Capability** 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device 10 = Asymmetric PAUSE toward link partner 01 = Symmetric PAUSE 00 = No PAUSE	R/W	01b
9	**100BASE-T4** 1 = 100BASE-T4 capable 0 = No 100BASE-T4 capability	RO	0b
8	**100BASE-TX Full Duplex** 1 = 100BASE-TX full duplex capable 0 = No 100BASE-TX full duplex capability	R/W	1b
7	**100BASE-TX Half Duplex** 1 = 100BASE-TX half duplex capable 0 = No 100BASE-TX half duplex capability	R/W	1b
6	**10BASE-T Full Duplex** 1 = 10BASE-T full duplex capable 0 = No 10BASE-T full duplex capability	R/W	1b
5	**10BASE-T Half Duplex** 1 = 10BASE-T half duplex capable 0 = No 10BASE-T half duplex capability	R/W	1b
4:0	**Selector Field** 00001 = IEEE 802.3	R/W	0x01

5.2.2.6 PHY Auto-Negotiation Link Partner Ability Register

Address: 0xN10A - 0xN10B Size: 16 bits
Port N: 1-5

PHY register 0x05.

Bits	Description	Type	Default
15	**Next Page** 1 = Next page capable 0 = No next page capability	RO	-
14	**Acknowledge** 1 = Link code word received from partner 0 = Link code word not yet received	RO	-
13	**Remote Fault** 1 = Remote fault detected 0 = No remote fault	RO	-
12	**RESERVED**	RO	-
11:10	**Pause (Flow Control) Capability** 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device 10 = Asymmetric PAUSE toward link partner 01 = Symmetric PAUSE 00 = No PAUSE	RO	-
9	**100BASE-T4** 1 = 100BASE-T4 capable 0 = No 100BASE-T4 capability	RO	-
8	**100BASE-TX Full Duplex** 1 = 100BASE-TX full duplex capable 0 = No 100BASE-TX full duplex capability	RO	-
7	**100BASE-TX Half Duplex** 1 = 100BASE-TX half duplex capable 0 = No 100BASE-TX half duplex capability	RO	-
6	**10BASE-T Full Duplex** 1 = 10BASE-T full duplex capable 0 = No 10BASE-T full duplex capability	RO	-
5	**10BASE-T Half Duplex** 1 = 10BASE-T half duplex capable 0 = No 10BASE-T half duplex capability	RO	-
4:0	**Selector Field** 00001 = IEEE 802.3	RO	-

5.2.2.7 PHY Auto-Negotiation Expansion Status Register

Address: 0xN10C - 0xN10D Size: 16 bits
Port N: 1-5

PHY register 0x06.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	0x000
4	**Parallel Detection Fault** 1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO LH	-
3	**Link Partner Next Page Able** 1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	-
2	**Next Page Able** 1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1b
1	**Page Received** 1 = New page received 0 = New page not received	RO LH	-
0	**Link Partner Auto-Negotiation Able** 1 = Link partner has auto-negotiation capability 0 =Link partner does not have auto-negotiation capability	RO	-

5.2.2.8 PHY Auto-Negotiation Next Page Register

Address: 0xN10E - 0xN10F Size: 16 bits
Port N: 1-5

PHY register 0x07.

Bits	Description	Type	Default
15	**Next Page** 1 = Additional next page(s) will follow 0 = Last page	R/W	0b
14	**RESERVED**	RO	0b
13	**Message Page** 1 = Message page 0 = Unformatted page	R/W	1b
12	**Acknowledge 2** 1 = Will comply with message 0 = Cannot comply with message	R/W	0b

Bits	Description	Type	Default
11	**Toggle** 1 = Previous value of transmitted link code word equaled logic one 0 = Previous value of transmitted link code word equaled logic zero	RO	0b
10:0	**Message Field**	R/W	0x001

5.2.2.9 PHY Auto-Negotiation Link Partner Next Page Ability Register

Address: 0xN110 - 0xN111 Size: 16 bits
Port N: 1-5

PHY register 0x08.

Bits	Description	Type	Default
15	**Next Page** 1 = Additional next page(s) will follow 0 = Last page	R/W	-
14	**Acknowledge** 1 = Successful receipt of link word 0 = No successful receipt of link word	RO	-
13	**Message Page** 1 = Message page 0 = Unformatted page	RO	-
12	**Acknowledge 2** 1 = Able to act on the information 0 = Not able to act on the information	RO	-
11	**Toggle** 1 = Previous value of transmitted link code word equaled logic zero 0 = Previous value of transmitted link code word equaled logic one	RO	-
10:0	**Message Field**	RO	-

5.2.2.10 PHY MMD Setup Register

Address: 0xN11A - 0xN11B Size: 16 bits
Port N: 1-5

PHY register 0x0D.

Bits	Description	Type	Default
15:14	**MMD Operation Mode** For the selected MMD device address (bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for the PHY MMD Data Register. 00 = Register 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	R/W	0x000
4:0	**MMD Device Address**	R/W	0x00

5.2.2.11 PHY MMD Data Register

Address: 0xN11C - 0xN11D Size: 16 bits
Port N: 1-5

PHY register 0x0E.

Bits	Description	Type	Default
15:0	**MMD R/W Index/Data** For the selected MMD device address (in the PHY MMD Setup Register, bits [4:0]): When the PHY MMD Setup Register bits [15:14] = 00, this register contains the read/write register access for the MDD device address. Otherwise, this register contains the read/write data value for the MMD device address and its selected register address Refer to the PHY MMD Setup Register bits [15:14] for descriptions of post increment reads and writes of this register for data operation.	R/W	0x0000

5.2.2.12 PHY Remote Loopback Register

Address: 0xN122 - 0xN123 Size: 16 bits
Port N: 1-5

PHY register 0x11.

Bits	Description	Type	Default
15:9	**RESERVED**	R/W	0x00
8	**Remote Loopback** Data received at the external pins of a port is looped back and sent out the same port, without passing through the internal switch fabric. For PHY ports, data is received on the RX+/- pins and transmitted out the TX+/- pins. For xMII ports, data is received on the TXD pins and transmitted on the RXD pins. 1 = Remote loopback 0 = Normal operation	R/W	0b
7:2	**RESERVED**	R/W	1111_01b
1	**RESERVED**	R/W RC	0b
0	**RESERVED**	RO	0b

5.2.2.13 PHY LinkMD Register

Address: 0xN124 - 0xN125 Size: 16 bits
Port N: 1-5

PHY register 0x12.

Bits	Description	Type	Default
15	**Cable Diagnostic Test Enable** Write value: 1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Disable cable diagnostic test. Read value: 1 = Cable diagnostic test is in progress. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	R/W, SC	0b
14:13	**RESERVED**	R/W	00b
12	**Cable Diagnostic Test Pair** Select the differential pair for testing: 0 = Differential pair TXP/TXM 1 = Differential pair RXP/RXM	R/W	0b
11:10	**RESERVED**	R/W	00b

Bits	Description	Type	Default
9:8	**Cable Diagnostic Status** 00 = Normal cable condition (no fault detected) 01 = Open cable fault detected 10 = Short cable fault detected 11 = Reserved	RO	00b
7:0	**RESERVED**	RO	0x00

5.2.2.14 PHY Digital PMA/PCS Status Register

Address: 0xN126 - 0xN127 Size: 16 bits
Port N: 1-5

PHY register 0x13.

Bits	Description	Type	Default
15:1	**RESERVED**	RO LH	0x0000
0	**100BASE-TX Link Status** 1 = Link is up 0 = Link is down	RO	-

5.2.2.15 Port RXER Count Register

Address: 0xN12A - 0xN12B Size: 16 bits
Port N: 1-5

PHY register 0x15.

Bits	Description	Type	Default
15:0	**RXER Counter** Count of receive frames with one or more symbol errors.	RO RC	0x0000

5.2.2.16 Port Interrupt Control / Status Register

Address: 0xN136 - 0xN137 Size: 16 bits
Port N: 1-5

PHY register 0x1B.

Bits	Description	Type	Default
15	**Jabber Interrupt Enable** 1 = Enable jabber interrupt 0 = Disable jabber interrupt	R/W	0b
14	**Receive Error Interrupt Enable** 1 = Enable receive error interrupt 0 = Disable receive error interrupt	R/W	0b
13	**Page Received Interrupt Enable** 1 = Enable page received interrupt 0 = Disable page received interrupt	R/W	0b
12	**Parallel Detect Fault Interrupt Enable** 1 = Enable parallel detect fault interrupt 0 = Disable parallel detect fault interrupt	R/W	0b
11	**Link Partner Acknowledge Interrupt Enable** 1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	R/W	0b
10	**Link Down Interrupt Enable** 1 = Enable link down interrupt 0 = Disable link down interrupt	R/W	0b
9	**Remote Fault Interrupt Enable** 1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	R/W	0b
8	**Link Up Interrupt Enable** 1 = Enable link up interrupt 0 = Disable link up interrupt	R/W	0b
7	**Jabber Interrupt** 1 = Jabber occurred 0 = Jabber did not occur	RO RC	0b
6	**Receive Error Interrupt** 1 = Receive error occurred 0 = Receive error did not occur	RO RC	0b
5	**Page Received Interrupt** 1 = Page receive occurred 0 = Page receive did not occur	RO RC	0b
4	**Parallel Detect Fault Interrupt** 1 = Parallel detect fault occurred 0 = Parallel detect fault did not occur	RO RC	0b

Bits	Description	Type	Default
3	**Link Partner Acknowledge Interrupt** 1 = Link partner acknowledge occurred 0 = Link partner acknowledge did not occur	RO RC	0b
2	**Link Down Interrupt** 1 = Link down occurred 0 = Link down did not occur	RO RC	0b
1	**Remote Fault Interrupt** 1 = Remote fault occurred 0 = Remote fault did not occur	RO RC	0b
0	**Link Up Interrupt** 1 = Link up occurred 0 = Link up did not occur	RO RC	0b

5.2.2.17 PHY Auto MDI / MDI-X Register

Address: 0xN138 - 0xN139 Size: 16 bits
Port N: 1-5

PHY register 0x1C.

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	0x00
7	**MDI Set** When Swap-Off bit is one, 1 = PHY is set to operate in MDI mode 0 = PHY is set to operate in MDI-X mode This bit has no function when Swap-Off is zero.	R/W	0b
6	**Swap-Off** 1 = Disable Auto MDI / MDI-X function 0 = Enable Auto MDI / MDI-X function (normal operation)	R/W	0b
5:0	**RESERVED**	R/W	0x00

5.2.2.18 PHY Control Register

Address: 0xN13E - 0xN13F Size: 16 bits
Port N: 1-5

PHY register 0x1F.

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	0x0
11:10	**RESERVED**	RO LH RC	00b
9	**Enable Jabber** 1 = Enable jabber counter 0 = Disable jabber counter	R/W	1b
8:7	**RESERVED**	R/W	10b
6	**RESERVED**	RO	-
5	**Speed Status 100BASE-TX** 1 = PHY final speed status is 100BASE-TX	RO	-
4	**Speed Status 10BASE-T** 1 = PHY final speed status is 10BASE-T	RO	-
3	**Duplex Status** 1 = Full duplex 0 = Half duplex	RO	-
2	**RESERVED**	RO	-
1	**RESERVED**	R/W RC	0b
0	**RESERVED**	RO RC	-

5.2.3 PORT N: PORT RGMII/MII/RMII CONTROL REGISTERS (0xN300 - 0xN3FF)

5.2.3.1 XMII Port Control 0 Register

Address: 0xN300 Size: 8 bits
Port N: 6-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6	**MAC Port Duplex** 1 = Port MAC interface operates in full-duplex mode 0 = Port MAC interface operates in half-duplex mode	R/W	1b
5	**MAC Port Transmit Flow Control Enable** 1 = Enable transmit flow control on this port 0 = Disable transmit flow control on this port	R/W	Note 5-5
4	**MAC Port Speed 10/100** This bit is ignored if bit 6 in the XMII Port Control 1 Register selects 1000 Mb/s. If bit 6 in the XMII Port Control 1 Register is one, then this bit determines the port speed: 1 = Port operates at 100 Mb/s 0 = Port operates at 10 Mb/s	R/W	1b
3	**MAC Port Receive Flow Control Enable** 1 = Enable receive flow control on this port 0 = Disable receive flow control on this port	R/W	Note 5-5
2:0	**RESERVED**	R/W	000b

Note 5-5 The default value of this field is determined by the **LED1_1** configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.2.3.2 XMII Port Control 1 Register

Address: 0xN301 Size: 8 bits
Port N: 6-7

Bits	Description	Type	Default
7	**RESERVED**	R/W	-
6	**Port Speed 1000** 1 = RGMII operates at 10 or 100 Mb/s, as determined by bit 4 in the XMII Port Control 0 Register 0 = RGMII operates at 1000 Mb/s	R/W	Note 5-6
5	**RESERVED**	R/W	0b
4	**RGMII Ingress Internal Delay (RGMII_ID_ig)** 1 = Minimum 1.5 ns delay is added to ingress RGMII clock 0 = No delay is added	R/W	0b
3	**RGMII Egress Internal Delay (RGMII_ID_eg)** 1 = Minimum 1.5 ns delay is added to egress RGMII clock 0 = No delay is added	R/W	1b
2	**MII / RMII Modes** **For MII interface:** 1 = The MII interface operates as a MAC device (receives clocks, etc.) 0 = The MII interface operates as a PHY device (drives clocks, etc.) **For RMII interface:** 1 = The 50 MHz RMII REFCLK is received at the RXC pin 0 = A 50 MHz RMII REFCLK is generated from the RXC pin	R/W	Note 5-7
1:0	**Port Interface Type Select** 00 = Interface is RGMII 01 = Interface is RMII 10 = Interface is MII 11 = Interface is MII	R/W	Note 5-8

Note 5-6 The default value of this field is determined by the **RXD6_0** (Port 6) or **RXD7_0** (Port 7) configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

Note 5-7 The default value of this field is determined by the **RXD6_1** (Port 6) or **RXD7_1** (Port 7) configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

Note 5-8 The default value of this field is determined by the **RXD6_[3:2]** (Port 6) or **RXD7_[3:2]** (Port 7) configuration strap value. Refer to Section 3.2.1, "Configuration Straps," on page 16 for additional information.

5.2.4 PORT N: PORT SWITCH MAC CONTROL REGISTERS (0xN400 - 0xN4FF)

5.2.4.1 Port MAC Control 0 Register

Address: 0xN400 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:4	**RESERVED**	RO	0x0
3	**RESERVED**	R/W	0b
2	**RESERVED**	RO	0b
1	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress traffic 0 = Disable broadcast storm protection for ingress traffic	R/W	0b
0	**Jumbo Packet Enable** 1 = Accept packets sizes up to 9000 bytes payload (excludes header and CRC) 0 = Standard payload limit of 1500 bytes applies	R/W	0b

5.2.4.2 Port MAC Control 1 Register

Address: 0xN401 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	R/W	0b
6	**RESERVED**	RO	0b
5:4	**RESERVED**	R/W	00b
3	**Back pressure Enable** Back pressure is used only for half duplex. Full duplex uses PAUSE frame flow control which is enabled separately. 1 = Enable port back pressure 0 = Disable port back pressure	R/W	0b
2:1	**RESERVED**	R/W	00b
0	**Pass All Frames** Bad frames (CRC error, too large, too small) are normally dropped. This feature allows them to be forwarded for mirroring purposes only. This bit does not affect filtering of flow control frames. To disable filtering of flow control frames, refer to the Switch MAC Control 4 Register. 1 = Enable 0 = Disable	R/W	0b

5.2.4.3 Port Ingress Rate Limit Control Register

Address: 0xN403 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6	**Port or Priority Based Ingress Rate Limiting** 1 = Ingress rate limiting is port based 0 = Ingress rate limiting is priority based	R/W	0b
5	**Ingress PPS Mode** 1 = Ingress rate limiting is based on number of packets (PPS mode enabled) 0 = Ingress rate limiting is based on number of bits (PPS mode disabled)	R/W	0b
4	**Ingress Rate Limit Flow Control Enable** To use this feature, flow control must also be enabled for this port. Refer to the XMII Port Control 0 Register for non-PHY ports, and the PHY Auto-Negotiation Advertisement Register for PHY ports. 1 = Flow control is asserted if the port's receive rate is exceeded 0 = Flow control is not asserted based on ingress rate limits	R/W	0b
3:2	**Ingress Limit Mode** These bits determine what kind of frames are limited and counted against ingress rate limiting. 00 = Count and limit all frames 01 = Count and limit broadcast, multicast and flooded unicast frames only 10 = Count and limit broadcast and multicast frames only 11 = Count and limit broadcast frames only	R/W	00b
1	**Count IFG Bytes** 1 = Each frame's minimum inter-frame gap (IFG) bytes (12 per frame) are included in ingress rate limiting calculations 0 = IFG byte count is not included	R/W	0b
0	**Count Preamble Bytes** Not valid when PPS mode is enabled (bit 5) 1 = Each frame's preamble bytes (8 per frame) are included in ingress rate limiting calculations 0 = Preamble byte count is not included	R/W	0b

5.2.4.4 Port Priority 0 Ingress Limit Control Register

Address: 0xN410 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 0 Frames** Reference Table 5-3 for code values. Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

TABLE 5-3: DATA RATE SELECTION TABLE FOR INGRESS AND EGRESS RATE LIMITING

Code	10Mbps		100Mbps		1000Mbps	
7 bits, decimal	**PPS**	**BPS**	**PPS**	**BPS**	**PPS**	**BPS**
7d’0	19.2k	10Mbps	192k	100Mbps	1.92M	1000Mbps
7d’1 – 7d’10	1.92k * code	1Mbps * code	1.92k * code	1Mbps * code	19.2k * code	1Mbps * code
7d’11 – 7d’100	–	10Mbps	1.92k * code	1Mbps * code	19.2k * code	10Mbps * code
7d’101	64	64kbps	64	640kbps	640	640kbps
7d’102	128	128kbps	128	1280kbps	1280	1280kbps
7d’103	256	192kbps	256	1920kbps	2560	1920kbps
7d’104	384	256kbps	384	256kbps	3840	2560kbps
7d’105	512	320kbps	512	320kbps	5120	3200kbps
7d’106	640	384kbps	640	384kbps	6400	3840kbps
7d’107	768	448kbps	768	448kbps	7680	4480kbps
7d’108	896	512kbps	896	512kbps	8960	5120kbps
7d’109	1024	576kbps	1024	576kbps	10,240	5760kbps
7d’110	1152	640kbps	1152	640kbps	11,520	6400kbps
7d’111	1280	704kbps	1280	704kbps	12,800	7040kbps
7d’112	1408	768kbps	1408	768kbps	14,080	7680kbps
7d’113	1536	832kbps	1536	832kbps	15,360	8320kbps
7d’114	1664	896kbps	1664	896kbps	16,640	8960kbps
7d’115	1792	960kbps	1792	960kbps	17,920	9600kbps

Note: PPS = Packets Per Second, BPS = Bits Per Second.

5.2.4.5 Port Priority 1 Ingress Limit Control Register

Address: 0xN411 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 1 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.6 Port Priority 2 Ingress Limit Control Register

Address: 0xN412 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 2 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.7 Port Priority 3 Ingress Limit Control Register

Address: 0xN413 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 3 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.8 Port Priority 4 Ingress Limit Control Register

Address: 0xN414 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 4 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.9 Port Priority 5 Ingress Limit Control Register

Address: 0xN415 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 5 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.10 Port Priority 6 Ingress Limit Control Register

Address: 0xN416 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 6 Frames** Note that the update will not take effect until the Port Priority 7 Ingress Limit Control Register is written.	R/W	0x00

5.2.4.11 Port Priority 7 Ingress Limit Control Register

Address: 0xN417 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Ingress Data Rate Limit for Priority 7 Frames**	R/W	0x00

5.2.4.12 Port Queue 0 Egress Limit Control Register

Address: 0xN420 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Egress Data Rate Limit for Queue 0 Frames** When egress rate limiting is configured to “port-based” via bit 3 of the Switch MAC Control 5 Register, only this register is used for setting. The Port Queue 1-3 Egress Limit Control Registers are used only for queue-based rate limiting. Note that the update will not take effect until the Port Queue 3 Egress Limit Control Register is written.	R/W	0x00

5.2.4.13 Port Queue 1 Egress Limit Control Register

Address: 0xN421 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Egress Data Rate Limit for Queue 1 Frames** Note that the update will not take effect until the Port Queue 3 Egress Limit Control Register is written.	R/W	0x00

5.2.4.14 Port Queue 2 Egress Limit Control Register

Address: 0xN422 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Egress Data Rate Limit for Queue 2 Frames** Note that the update will not take effect until the Port Queue 3 Egress Limit Control Register is written.	R/W	0x00

5.2.4.15 Port Queue 3 Egress Limit Control Register

Address: 0xN423 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Egress Data Rate Limit for Queue 3 Frames**	R/W	0x00

5.2.5 PORT N: PORT SWITCH MIB COUNTERS REGISTERS (0xN500 - 0xN5FF)

Thirty MIB counters are provided for each port. They are accessed via the following two indirect registers. MIB Counters are read-clear. Refer to Section 5.3.6, "Management Information Base (MIB) Counters" for additional details.

Note: The Switch MIB Control Register contains two additional bits for global control of MIB counters.

5.2.5.1 Port MIB Control and Status Register

Address: 0xN500 - 0xN503 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31	**MIB Counter Overflow Indication** 1 = Counter has overflowed 0 = Counter has not overflowed	RO	0b
30:26	**RESERVED**	RO	0x00
25	**MIB Read Enable / Count Valid** Set this bit to '1' to initiate a counter read. When the counter read is complete and the count value is available in the MIB Counter Value, this bit will automatically clear to '0'.	R/W SC	0b
24	**MIB Flush and Freeze Enable** Refer to the Switch MIB Control Register for the associated global MIB control bits for flushing and freezing port counters. 1 = Enable MIB counter flush and freeze function for this port 0 = Disable MIB counter flush and freeze function for this port	R/W	0b
23:16	**MIB Index**	R/W	0x00
15:4	**RESERVED**	RO	0x000
3:0	**MIB Counter Value [35:32]**	RO	0x0

5.2.5.2 Port MIB Data Register

Address: 0xN504 - 0xN507 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:0	**MIB Counter Value [31:0]**	RO	0x0000

5.2.6 PORT N: PORT SWITCH ACL CONTROL REGISTERS (0xN600 - 0xN6FF)

An Access Control List (ACL) Table is provided for each port. It is accessed via the following two indirect registers. Refer to Section 5.3.5, "Access Control List (ACL) Table" for additional details.

5.2.6.1 Port ACL Access 0 Register

Address: 0xN600 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:4	**RESERVED**	RO	0x0
3:0	**First Rule Number (FRN)**	R/W	0x0

5.2.6.2 Port ACL Access 1 Register

Address: 0xN601 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:6	**RESERVED**	R/W	00b
5:4	**Mode** 00 = No action taken 01 = Layer 2 MAC header filtering 10 = Layer 3 IP address filtering 11 = Layer 4 TCP port number / IP protocol filtering	R/W	00b
3:2	**Enable**	R/W	00b
1	**Source / Destination** 1 = Source 0 = Destination	R/W	0b
0	**Compare Equal** 1 = Match if the compared values are equal 0 = Match if the compared values are not equal	R/W	0b

5.2.6.3 Port ACL Access 2 Register

Address: 0xN602 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [47:40]**	R/W	0x00

5.2.6.4 Port ACL Access 3 Register

Address: 0xN603 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [39:32]**	R/W	0x00

5.2.6.5 Port ACL Access 4 Register

Address: 0xN604 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [31:24]**	R/W	0x00

5.2.6.6 Port ACL Access 5 Register

Address: 0xN605 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [23:16]**	R/W	0x00

5.2.6.7 Port ACL Access 6 Register

Address: 0xN606 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [15:8]**	R/W	0x00

5.2.6.8 Port ACL Access 7 Register

Address: 0xN607 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**MAC Address [7:0]**	R/W	0x00

5.2.6.9 Port ACL Access 8 Register

Address: 0xN608 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**EtherType [15:8]**	R/W	0x00

5.2.6.10 Port ACL Access 9 Register

Address: 0xN609 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**EtherType [7:0]**	R/W	0x00

5.2.6.11 Port ACL Access A Register

Address: 0xN60A Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:6	**Priority Mode (PM)**	R/W	00b
5:3	**Priority**	R/W	00_0b
2	**Remark Priority Enable (RPE)**	R/W	0b
1:0	**Remark Priority [2:1]** The two MSB of the 3-bit Remark Priority field. Refer to the Port ACL Access B Register for the LSB.	R/W	00b

5.2.6.12 Port ACL Access B Register

Address: 0xN60B Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**Remark Priority [0]** The LSB of the 3-bit Remark Priority field. Refer to the Port ACL Access B Register for the MSB.	R/W	0b
6:5	**Map Mode (MM)**	R/W	00b
4:0	**RESERVED**	R/W	0b

5.2.6.13 Port ACL Access C Register

Address: 0xN60C Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**RESERVED**	R/W	0x00

5.2.6.14 Port ACL Access D Register

Address: 0xN60D Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	R/W	0b
6:0	**Port Forward Map** Each bit corresponds to a forwarding port. Bit 0 corresponds to port 1, Bit 1 corresponds to port 2, etc. 1 = enable forwarding to that port 0 = do not forward to that port	R/W	000_0000b

5.2.6.15 Port ACL Access E Register

Address: 0xN60E Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Ruleset [15:8]**	R/W	0x00

5.2.6.16 Port ACL Access F Register

Address: 0xN60F Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Ruleset [7:0]**	R/W	0x00

5.2.6.17 Port ACL Byte Enable MSB Register

Address: 0xN610 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Byte Enable [15:8]** Each bit enables accessing one of the ACL bytes when a read or write is initiated by writing to the Port ACL Byte Enable LSB Register. Bit 0 applies to the Port ACL Access 7 Register Bit 1 applies to the Port ACL Access 6 Register, etc. Bit 7 applies to the Port ACL Access 0 Register 1 = Byte is selected for read/write 0 = Byte is not selected	R/W	0x00

5.2.6.18 Port ACL Byte Enable LSB Register

Address: 0xN611 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:0	**Byte Enable [7:0]** Each bit enables accessing one of the ACL bytes when a read or write is initiated by writing to the Port ACL Byte Enable LSB Register. Bit 0 applies to the Port ACL Access F Register Bit 1 applies to the Port ACL Access E Register, etc. Bit 7 applies to the Port ACL Access 8 Register 1 = Byte is selected for read/write 0 = Byte is not selected	R/W	0x00

5.2.6.19 Port ACL Access Control 0 Register

Address: 0xN612 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**RESERVED**	R/O	0b
6	**Write Status** 1 = Write operation is complete 0 = Write operation is not complete	RO	1b
5	**Read Status** 1 = Read operation is complete 0 = Read operation is not complete; continue polling until this bit is set before reading results registers	RO	1b
4	**Write / Read** 1 = Write 0 = Read	R/W	0b
3:0	**ACL Index**	R/W	0x0

5.2.7 PORT N: PORT SWITCH INGRESS CONTROL REGISTERS (0xN800 - 0xN8FF)

5.2.7.1 Port Mirroring Control Register

Address: 0xN800 Size: 8 bits
Port N: 1-7

This register contains the port controls for port mirroring. The Global Port Mirroring and Snooping Control Register must also be properly configured.

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6	**Receive Sniff** 1 = All packets received on this port are designated as “monitored packets” and will be forwarded to the designated “sniffer port”. 0 = No receive monitoring.	R/W	0b
5	**Transmit Sniff** 1 = All packets transmitted on this port are designated as “monitored packets” and will be forwarded to the designated “sniffer port”. 0 = No transmit monitoring.	R/W	0b
4:2	**RESERVED**	RO	0_00b
1	**Sniffer Port** 1 = This port is designated as the sniffer port and will transmit monitored packets. 0 = Not a sniffer port. Normal operation.	R/W	0b
0	**RESERVED**	RO	0b

5.2.7.2 Port Priority Control Register

Address: 0xN801 Size: 8 bits
Port N: 1-7

To achieve the desired functionality, do not set more than one bit at a time in this register.

Bits	Description	Type	Default
7	**Highest Priority** 1 = Highest priority selected 0 = Highest priority not selected	R/W	0b
6	**OR’ed Priority** 1 = All available priority OR’ed 0 = All available priority not OR’ed	R/W	0b
5	**RESERVED**	RO	0b
4	**MAC Address Priority Classification** 1 = Enable MAC address priority classification for ingress packets on port 0 = Disable MAC address classification	R/W	0b

Bits	Description	Type	Default
3	**VLAN Priority Classification** 1 = Enable VLAN priority classification for ingress packets on port 0 = Disabled VLAN classification	R/W	0b
2	**802.1p Priority Classification** 1 = Enable 802.1p priority classification for ingress packets on port 0 = Disable 802.1p priority classification	R/W	0b
1	**Diffserv Priority Classification** 1 = Enable Diffserv priority classification for ingress packets on port 0 = Disable Diffserv priority classification	R/W	0b
0	**ACL Priority Classification** 1 = Enable ACL priority classification for ingress packets on port 0 = Disable ACL priority classification	R/W	0b

5.2.7.3 Port Ingress MAC Control Register

Address: 0xN802 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**User Priority Ceiling** 1 = If a packet's "user priority field" is greater than the "user priority field" in the port default tag register, replace the packet's user priority field with the user priority field in the port default tag from the Port Default Tag 0 Register. 0 = Do not replace the user priority field at this port.	R/W	0b
6:5	**RESERVED**	RO	0b
4	**Discard Untagged Packets** This bit should be left as 0 for the host port. 1 = Any ingress packet at this port without an IEEE 802.1Q tag is discarded. 0 = Do not discard.	R/W	0b
3	**Discard Tagged Packets** 1 = Any ingress packet at this port with an IEEE 802.1Q tag is discarded. 0 = Do not discard.	R/W	0b
2:0	**Port Default Priority Classification** If Diffserv classification, 802.1p classification and VLAN classification are not enabled or fail to classify, ingress packets at this port will be classified with the priority specified here. Possible values are 0 to 7.	R/W	000b

5.2.7.4 Port Authentication Control Register

Address: 0xN803 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_0b
2	**Access Control List (ACL) Enable** 1 = enable 0 = enable	R/O	0b
1:0	**Authentication Mode** 00 = Pass Mode. Authentication is disabled. When ACL is enabled, all traffic that misses the ACL rules is forwarded; otherwise ACL actions apply. 01 = Block Mode. Authentication is enabled. When ACL is enabled, all traffic that misses the ACL rules is blocked; otherwise ACL actions apply. 10 = Trap Mode. Authentication is enabled. All traffic is forwarded to the host port. When ACL is enabled, all traffic that misses the ACL rules is blocked; otherwise ACL actions apply. 11 = Reserved	R/W	00b

5.2.7.5 Port Pointer Register

Address: 0xN804 - 0xN807 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:19	**RESERVED**	RO	0x0000
18:16	**Port Index** Used to point to the indirect mapping locations for the 7 ports	R/W	000b
15:2	**RESERVED**	RO	0x0000
1:0	**Queue Pointer** Used to point to the indirect mapping locations for the 4 queues	R/W	00b

5.2.7.6 Port Priority to Queue Mapping Register

Address: 0xN808 - 0xN80B Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:28	Regenerated priority (queue) value for priority 7. The 2 most significant bits are reserved.	R/W	xx11b
27:24	Regenerated priority (queue) value for priority 6. The 2 most significant bits are reserved.	R/W	xx11b
23:20	Regenerated priority (queue) value for priority 5. The 2 most significant bits are reserved.	R/W	xx10b
19:16	Regenerated priority (queue) value for priority 4. The 2 most significant bits are reserved.	R/W	xx10b
15:12	Regenerated priority (queue) value for priority 3. The 2 most significant bits are reserved.	R/W	xx01b
11:8	Regenerated priority (queue) value for priority 2. The 2 most significant bits are reserved.	R/W	xx01b
7:4	Regenerated priority (queue) value for priority 1. The 2 most significant bits are reserved.	R/W	xx00b
3:0	Regenerated priority (queue) value for priority 0. The 2 most significant bits are reserved.	R/W	xx00b

5.2.7.7 Port Police Control Register

Address: 0xN80C - 0xN80F Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
31:12	**RESERVED**	RO	0x00000
11	**Dropped Color** 1 = Color packet PMON holds dropped packets of that color 0 = Color packet PMON holds all packets of that color	R/W	0b
10	**Drop All** 1 = All packets are dropped while max threshold is exceeded in PM WRED 0 = Drop packet based on WRED_PM_PROB_MULTIPLIER	R/W	0b
9:8	**Packet Type** PMON packet type to be read for the connection from Queue Pointer of the port pointed by Port Index 11 = WRED_PMON holds the number of RED packets while read 10 = WRED_PMON holds the number of YELLOW packets while read 01 = WRED_PMON holds the number of GREEN packets while read 00 = WRED_PMON holds the number of dropped packets while read	R/W	00b
7	**Port Based Policing** 1 = Policing is per-port per-queue based 0 = Policing is per-queue based only, Port Index = 0 is used to set aggregated CIR, PIR for each queue	R/W	0b
6:5	**NONDSCP_COLOR** Color of non-IP frame for color aware	R/W	01b
4	**Color Mark Enable** 1 = DSCP color mark enable 0 = DSCP color mark disable	R/W	0b
3	**Color Remap Enable** 1 = DSCP color remap enable for color aware 0 = DSCP color remap disable, use DSCP color	R/W	0b
2	**Drop SRP** 1 = Allow drop SRP packets while WRED is enabled 0 = Don’t allow drop SRP packet while WRED is enabled	R/W	0b
1	**Police Mode** This bit sets the policing modes for the queue if policing is enabled 1 = Color blind 0 = Color aware mode	R/W	0b
0	**Police Enable** 1 = Enable policing and WRED 0 = Disable policing and WRED	R/W	0b

5.2.7.8 Port Police Queue Rate Register

Address: 0xN820 - 0xN823 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:16	**Committed Information Rate** Specifies the committed information rate for the connection from the Queue Pointer of the port pointed by the Port index.	R/W	0x1000
15:0	**Peak Information Rate** Specifies the queue's peak information rate for the connection from the Queue Pointer of the port pointed by the Port index.	R/W	0x2000

5.2.7.9 Port Police Queue Burst Size Register

Address: 0xN824 - 0xN827 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:16	**Committed Burst Size** Specifies the queue's committed burst size in bytes that is supported for the connection from the Queue Pointer of the port pointed by the Port index.	R/W	0x1000
15:0	**Peak Information Rate** Specifies the queue's peak burst size in bytes that is supported for the connection from the Queue Pointer of the port pointed by the Port index.	R/W	0x3000

5.2.7.10 Port WRED Packet Memory Control Register 0

Address: 0xN830 - 0xN833 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:27	**RESERVED**	RO	00000b
26:16	**WRED Packet Memory Maximum Threshold**	R/W	0x400
15:11	**RESERVED**	RO	00000b
10:0	**WRED Packet Memory Minimum Threshold**	R/W	0x080

5.2.7.11 Port WRED Packet Memory Control Register 1

Address: 0xN834 - 0xN837 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:27	**RESERVED**	RO	00000b
26:16	**WRED Packet Memory Probability Multiplier**	R/W	0x020
15:11	**RESERVED**	RO	00000b
10:0	**WRED Packet Memory Average Queue Size**	R	-

5.2.7.12 Port WRED Queue Control Register 0

Address: 0xN840 - 0xN843 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:27	**RESERVED**	RO	00000b
26:16	**WRED Maximum Queue Threshold** WRED maximum threshold for the connection from the Queue Pointer of the port pointed to by the Port index.	R/W	0x080
15:11	**RESERVED**	RO	00000b
10:0	**WRED Minimum Queue Threshold** WRED minimum threshold for the connection from the Queue Pointer of the port pointed to by the Port index.	R/W	0x009

5.2.7.13 Port WRED Queue Control Register 1

Address: 0xN844 - 0xN847 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:27	**RESERVED**	RO	00000b
26:16	**WRED Queue Probability Multiplier** Probability multiplier for the connection from the Queue Pointer of the port pointed to by the Port index.	R/W	0x010
15:11	**RESERVED**	RO	00000b
10:0	**WRED Packet Memory Average Queue Size** Average queue size for the connection from the Queue Pointer of the port pointed to by the Port index.	R	-

5.2.7.14 Port WRED Queue Performance Monitor Control Register

Address: 0xN848 - 0xN84B Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31	**Random Drop Enable** 1 = Random Drop enabled 0 = Random Drop disabled	R/W	0b
30	**PMON Flush** 1 = PMON counters are flushed. This is a low to high edge triggered clear. 0 = No activity	R/W	0x010
29	**GYR Drop Disable** 1 = Drop GREEN/YELLOW/RED is disabled 0 = Drop GREEN/YELLOW/RED is enabled	R/W	0b
28	**YR Drop Disable** 1 = Drop YELLOW/RED is disabled 0 = Drop YELLOW/RED is enabled	R/W	0b
27	**R Drop Disable** 1 = Drop RED is disabled 0 = Drop RED is enabled	R/W	0b
26	**Drop All** 1 = Drop all packets wile the max threshold is exceeded 0 = Drop based on WRED Queue Probability Multiplier	R/W	0b
25:24	**RESERVED**	RO	00b
23:0	**Packet Event Counter** Packer event count for the connection from the Queue Pointer of the port pointed to by the Port index.	R	0x00000

5.2.8 PORT N: PORT SWITCH EGRESS CONTROL REGISTERS (0xN900 - 0xN9FF)

5.2.8.1 Port Transmit Queue Index Register

Address: 0xN900 - 0xN903 Size: 32 bits
Port N: 1-7

This register holds an index value that is used when accessing several registers that follow. This register may be accessed as an 8-bit register, with bits [7:0] located at address 0xN903.

Bits	Description	Type	Default
31:2	**RESERVED**	RO	0x00000000
1:0	**Queue Index** Points to the queue number for subsequent queue configuration registers.	R/W	00

5.2.8.2 Port Transmit Queue PVID Register

Address: 0xN904 - 0x907 Size: 32 bits
Port N: 1-7

This register may be accessed as an 8-bit register, with bits [7:0] located at address 0xN903.

Bits	Description	Type	Default
31:1	**RESERVED**	RO	0x00000000
0	**Port VID Replacement** 1 = For any egress packet with a non-zero VLAN ID, replace the VID with the port default VID from the Port Default Tag 0 Register and Port Default Tag 1 Register. If double tagging is enabled, it is the ISP tag ID that will be replaced. 0 = Do not replace the VID.	R/W	0b

5.2.8.3 Port Transmit Queue Control 0 Register

Address: 0xN914 Size: 8 bits
Port N: 1-7

This register is indexed. Settings are applied on a per-queue and per-port basis. Specify the target queue number in the Port Transmit Queue Index Register before accessing this register.

Bits	Description	Type	Default
7:6	**Scheduler Mode** Determines the egress scheduling policy when 2 or 4 transmit queues are enabled. 00 = Strict Priority. All packets in queue 3 are transmitted before any packets from any lower number queue will be transmitted. All packets in queue 2 are transmitted before any packets from any lower number queue, etc.. 10 = Weighted Round Robin (WRR). As determined by the weight values in the (queue indexed) Port Transmit Queue Control 1 Register, a limited number of packets are transmitted from a queue before the next queue is serviced. All queues are serviced in turn. 01 and 11 = RESERVED	R/W	10b
5:4	**Shaper Mode** Determines the egress traffic shaper used. 00 = No shaping. 01 = Credit based shaper (CBS) as defined in IEEE 802.1Qav for AVB 10 = Time aware shaper (TAS) per IEEE 802.1Qbv for TSN 11 = RESERVED	R/W	00b
3:0	**RESERVED**	RO	0000b

5.2.8.4 Port Transmit Queue Control 1 Register

Address: 0xN915 Size: 8 bits
Port N: 1-7

This register is indexed. Settings are applied on a per-queue and per-port basis. Specify the target queue number in the Port Transmit Queue Index Register before accessing this register.

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Queue Weight for WRR Scheduling** During weighted round robin (WRR) scheduling, this value specifies the number of packets that may be transmitted from the particular queue before the next queue is serviced. These values are not relevant when the port is configured for a single egress queue. Do not assign 0 to any queue. Example values for a 4-queue configuration are 8 (for queue 3), 4 (for queue 2), 2 (for queue1) and 1 (for queue 0).	R/W	0000001

5.2.8.5 Port Transmit Credit Shaper Control 0 Register

Address: 0xN916 - 0xN917 Size: 16 bits
Port N: 1-

This register is indexed. Settings are applied on a per-queue and per-port basis. Specify the target queue number in the Port Transmit Queue Index Register before accessing this register.

Bits	Description	Type	Default
15:0	**Port Queue Credit High Water Mark** Shaper credit high water mark in bytes	R/W	0x0534

5.2.8.6 Port Transmit Credit Shaper Control 1 Register

Address: 0xN918 - 0xN919 Size: 16 bits
Port N: 1-

This register is indexed. Settings are applied on a per-queue and per-port basis. Specify the target queue number in the Port Transmit Queue Index Register before accessing this register.

Bits	Description	Type	Default
15:0	**Port Queue Credit Low Water Mark** Shaper credit low water mark in bytes	R/W	0x05F2

5.2.8.7 Port Transmit Credit Shaper Control 2 Register

Address: 0xN91A - 0xN91B Size: 16 bits
Port N: 1-

This register is indexed. Settings are applied on a per-queue and per-port basis. Specify the target queue number in the Port Transmit Queue Index Register before accessing this register.

Bits	Description	Type	Default
15:0	**Port Queue Credit Increment** Shaper credit increment, 12.5%	R/W	0x2000

5.2.8.8 Port Time Aware Shaper Control Register

Address: 0xN920 Size: 8 bits
Port N: 1-

Bits	Description	Type	Default
7	**Cut-Through Enable** 1 = Enable TAS cut-through 0 = Disable TAS cut-through	R/W	0b
6	**Restricted TAS** 1 = TAS packets will not be allowed to transmit out until the OPEN (scheduled) period when this bit is set to 1. They (either store & forward or cut-through) will be queued up. 0 = TAS packets will be allowed to transmit at any time	R/W	0b
5:2	**RESERVED**	RO	0000b
1:0	**Reference Time Select** 11 = Start t0 when reference time is crossed 10 = Repeat t0 on PTP pps (pulse per second) 01 = Free-running, repeats t0 based on internal 1 second pulse 00 = No reference	R/W	00b

5.2.8.9 Port Time Aware Shaper Event Index Register

Address: 0xN923 Size: 8 bits
Port N: 1-

Bits	Description	Type	Default
7	**RESERVED**	RO	0b
6:0	**Event Index**	R/W	0000000b

5.2.8.10 Port Time Aware Shaper Event Register

Address: 0xN924 - 0xN927 Size: 32 bits
Port N: 1-

Bits	Description	Type	Default
31:29	**Event** Event code: 111 = Repeat event 011-110 = RESERVED 010 = Scheduled open even 001 = Guard band start event 000 = Scheduled closed event	R/W	000b
28:0	**Time** Cycle count of system clock	R/W	0x000

5.2.9 PORT N: PORT SWITCH QUEUE MANAGEMENT CONTROL REGISTERS (0xNA00 - 0xNAFF)

5.2.9.1 Port Control 0 Register

Address: 0xNA00 - 0xNA03 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
32:2	**RESERVED**	RO	0x0000000
1:0	**Drop Mode** 00 = No drop, issue flow control to this port when destination is in congestion state. 01 = Drop packets with priority 0 sourced from this port when destination is in congestion state and disable the flow control to this port. 10 = Drop packets with priority 0, 1 sourced from this port when destination is in congestion state and disable the flow control to this port. 11 = Drop packets with priority 0, 1, 2 sourced from this port when destination is in congestion state and disable the flow control to this port.	R/W	00b

5.2.9.2 Port Control 1 Register

Address: 0xNA04 - 0xNA07 Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:7	**RESERVED**	RO	0x0000000
6:0	**Port VLAN Membership** Each bit corresponds to a device port. This feature does not utilize VLAN tags or the VLAN Table, and is unrelated to tag-based VLAN functions. Also refer to bit 1 in the Queue Management Control 0 Register. Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Frames may be forwarded to the corresponding port 0 = Frames are blocked from being forwarded to corresponding port	R/W	0x7F

5.2.10 PORT N: PORT SWITCH ADDRESS LOOKUP CONTROL REGISTERS (0xNB00 - 0xNBFF)

5.2.10.1 Port Control 2 Register

Address: 0xNB00 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7	**Null VID Lookup Enable** How to handle tagged packets with VID = 0. 1 = Non-standard operation. VLAN Table lookup using VID = 0. 0 = Standard operation. VLAN Table lookup using the port default VID (Port Default Tag 0 Register and Port Default Tag 1 Register)	R/W	0b
6	**Ingress VLAN Filtering** 1 = Discard packets whose VID port membership in the VLAN Table does not include the ingress port 0 = No ingress filtering	R/W	0b
5	**Discard Non-PVID Packet** 1 = Discard packets whose VID does not match the ingress port default VID 0 = Do not compare VID to the port default VID	R/W	0b
4	**MAC Based 802.1X Enable** 1 = Enable MAC based 802.1X authentication in lookup engine 0 = Only use ACL (if enabled) to perform MAC based authentication	R/W	0b
3	**Self-Address Filtering – Port Enable** The source address of received packets is compared to the MAC address in the Switch MAC Address 0 Register through Switch MAC Address 5 Register, and the packet is dropped if there is a match. Both this port enable bit and the global enable bit in the Switch Lookup Engine Control 1 Register must be set to enable self-address filtering. 1 = Enable self-address filtering for this port. 0 = Disable self-address filtering for this port.	R/W	0b
2	**RESERVED**	RO	0b
1	**RESERVED**	R/W	0b
0	**RESERVED**	RO	0b

5.2.10.2 Port MSTP Pointer Register

Address: 0xNB01 Size: 8 bits
Port N: 1-7

Bits	Description	Type	Default
7:3	**RESERVED**	R/W	0000_0b
2:0	**MSTP Pointer** Points to one of the 8 MSTPs. It is used as an index when reading or writing the Port MSTP State Register.	R/W	000b

5.2.10.3 Port MSTP State Register

Address: 0xNB04 Size: 8 bits
Port N: 1-7

There are eight MSTPs, and the MSTP Pointer in the Port MSTP Pointer Register is used as an index to select a particular MSTP when reading or writing this register.

Bits	Description	Type	Default
7:3	**RESERVED**	RO	0000_0b
2	**Port Transmit Enable** 1 = Enable packet transmission on the port 0 = Disable packet transmission on the port	R/W	1b
1	**Port Receive Enable** 1 = Enable packet reception on the port 0 = Disable packet reception on the port	R/W	1b
0	**Port Learning Disable** 1 = Disable switch address learning on the port 0 = Enable switch address learning on the port	R/W	0b

5.2.11 PORT N: PORT SWITCH PTP CONTROL REGISTERS (0xNC00 - 0xNCFF)

5.2.11.1 Port PTP Receive Latency Register

Address: 0xNC00 - 0xNC01 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N RX Latency in Nanoseconds (PTP_RX_LATENCY[15:0])** This field is used to set the fixed receive delay value from the port N wire to the RX timestamp reference point. The default value is 415ns.	R/W	0x019F

5.2.11.2 Port PTP Transmit Latency Register

Address: 0xNC02 - 0xNC03 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N TX Latency in Nanoseconds (PTP_TX_LATENCY[15:0])** This field is used to set the fixed transmit delay value from the port N TX timestamp to the wire. The default value is 45ns.	R/W	0x002D

5.2.11.3 Port PTP Asymmetry Correction Register

Address: 0xNC04 - 0xNC05 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15	**PTP Port N Asymmetry Correction Sign Bit (PTP_ASYM_COR_SIGN)** 1 = The magnitude in the PTP_ASM_COR field of this register is negative. 0 = The magnitude in the PTP_ASM_COR field of this register is positive.	R/W	0b
14:0	**PTP Port N Asymmetry Correction in Nanoseconds (PTP_ASYM_COR)** This field is used to set the fixed asymmetry value to add in the correction field for ingress Sync and Pdelay_Resp or to subtract from the correction field for egress Delay_Req and Pdelay_Req.	R/W	0x0000

5.2.11.4 Port PTP Egress Timestamp for Request and Delay High Word Register

Address: 0xNC08 - 0xNC09 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Pdelay_Req and Delay_Req in Nanoseconds (XDLY_REQ_TS[31:16])** This field contains the Port N egress timestamp high-word value for Pdelay_Req and Delay_Req frames in nanoseconds.	RO	0x0000

5.2.11.5 Port PTP Egress Timestamp for Request and Delay Low Word Register

Address: 0xNC0A - 0xNC0B Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Pdelay_Req and Delay_Req in Nanoseconds (XDLY_REQ_TS[15:0])** This field contains the Port N egress timestamp low-word value for Pdelay_Req and Delay_Req frames in nanoseconds.	RO	0x0000

5.2.11.6 Port PTP Egress Timestamp for Sync High Word Register

Address: 0xNC0C - 0xNC0D Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Sync in Nanoseconds (SYNC_TS[31:16])** This field contains the Port N egress timestamp high-word value for the Sync frame in nanoseconds.	RO	0x0000

5.2.11.7 Port PTP Egress Timestamp for Sync Low Word Register

Address: 0xNC0E - 0xNC0F Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Sync in Nanoseconds (SYNC_TS[15:16])** This field contains the Port N egress timestamp low-word value for the Sync frame in nanoseconds.	RO	0x0000

5.2.11.8 Port PTP Egress Timestamp for PDelay_Resp High Word Register

Address: 0xNC10 - 0xNC11 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Pdelay_Resp in Nanoseconds (PDLY_TS[31:16])** This field contains the Port N egress timestamp high-word value for the Pdelay_Resp frame in nanoseconds.	RO	0x0000

5.2.11.9 Port PTP Egress Timestamp for PDelay_Resp Low Word Register

Address: 0xNC12 - 0xNC13 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15:0	**PTP Port N Egress Timestamp for Pdelay_Resp in Nanoseconds (PDLY_TS[15:0])** This field contains the Port N egress timestamp low-word value for the Pdelay_Resp frame in nanoseconds.	RO	0x0000

5.2.11.10 Port PTP Timestamp Interrupt Status Register

Address: 0xNC14 - 0xNC15 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15	**Port N Egress Timestamp for Sync Frame Interrupt Status (TS_SYNC_INT_STATUS)** When this bit is set to 1, it indicates that the egress timestamp is available from Port N for the Sync frame. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Status bit in the Port Interrupt Status Register.	R/W1C	0b
14	**Port N Egress Timestamp for Pdelay_Req and Delay_Req Frames Interrupt Status (TS_PDLY_REQ_INT_STATUS)** When this bit is set to 1, it indicates that the egress timestamp is available from Port N for the Pdelay_Req and Delay_Req frames. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Status bit in the Port Interrupt Status Register.	R/W1C	0b
13	**Port N Egress Timestamp for Pdelay_Resp Frame Interrupt Status (TS_PDLY_RESP_INT_STATUS)** When this bit is set to 1, it indicates that the egress timestamp is available from Port N for the Pdelay_Resp frame. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Status bit in the Port Interrupt Status Register.	R/W1C	0b
12:0	**RESERVED**	RO	0x000

5.2.11.11 Port PTP Timestamp Interrupt Enable Register

Address: 0xNC16 - 0xNC17 Size: 16 bits
Port N: 1-7

Bits	Description	Type	Default
15	**Port N Egress Timestamp for Sync Frame Interrupt Enable (TS_SYNC_INT_ENB)** When this bit is set to 1, the egress timestamp interrupt from Port N for the Sync frame is enabled. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Enable bit in the Port Interrupt Mask Register.	R/W	0b
14	**Port N Egress Timestamp for Pdelay_Req and Delay_Req Frames Interrupt Enable (TS_PDLY_REQ_INT_ENB)** When this bit is set to 1, the egress timestamp interrupt from Port N for the Pdelay_Req and Delay_Req frames is enabled. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Enable bit in the Port Interrupt Mask Register.	R/W	0b
13	**Port N Egress Timestamp for Pdelay_Resp Frame Interrupt Enable (TS_PDLY_RESP_INT_ENB)** When this bit is set to 1, the egress timestamp interrupt from Port N for the Pdelay_Resp frame is enabled. This bit is logical OR'ed together with the rest of the bits in this register and the output is shown as the PTP Interrupt Enable bit in the Port Interrupt Mask Register.	R/W	0b
12:0	**RESERVED**	RO	0x000

5.2.11.12 Port PTP Link Delay Register

Address: 0xNC18 - 0xNC1B Size: 32 bits
Port N: 1-7

Bits	Description	Type	Default
31:0	**PTP Port N Link Delay in nanoseconds** This register is used to set the link delay value between port N and the link partner port.	R/W	0x0000_0000

5.3 Tables and MIB Counters (Access)

Indirect address and data registers are used to access the various tables and counters:

- Address Lookup (ALU) Table
- Static Address Table
- Reserved Multicast Address Table
- VLAN Table
- Access Control List (ACL) Table
- Management Information Base (MIB) Counters

5.3.1 ADDRESS LOOKUP (ALU) TABLE

The Address Lookup Table is the largest of three tables used for MAC address lookup. It supports both dynamic and static MAC address entries. In response to a destination address (DA) lookup, all tables are searched to make a packet forwarding decision. In response to a source address (SA) lookup, only this table is searched for aging, migration and learning of the dynamic entries.

It is suggested that static address entries be programmed to the Static Address Table. When that table is full, additional static address entries may be programmed into this table. Static entries will not be aged out.

A static DA lookup result (in either this table or the Static Address Table) takes precedence over the dynamic DA lookup result.

This table is a 4-way associative memory, with 1K buckets, for a total of 4K entries. In normal operation, the MAC address (and optionally the FID) are hashed to generate a 10-bit index. The 10-bit index specifies a bucket of up to 4 entries, but the entries within each bucket are not individually addressable. A new entry can be added to a bucket if the bucket contains 3 or fewer valid entries. Once a bucket is full with 4 valid entries, any new entry will overwrite the least-recently-used dynamic entry.

If a bucket contains 2 or 3 static entries, adding an additional static entry to that bucket will generate an Almost Full interrupt. (Refer to the Address Lookup Table Interrupt Register and Global Interrupt Status Register). Once the interrupt is generated, the 12-bit absolute address of the new static entry will be available for reading in the Address Lookup Table Entry Index 0 Register bits [11:0].

If a bucket is full with 4 static entries, attempting to write an additional static entry will fail and will result in a Write Fail Interrupt. Once the interrupt is generated, the 10-bit index of the full bucket will be available for reading in the Address Lookup Table Entry Index 0 Register bits [9:0].

A bucket with 4 static entries will also block any dynamic entries from being learned. Such a failure will generate a Learn Fail Interrupt. Once the interrupt is generated, the 10-bit index of the full bucket will be available for reading in the Address Lookup Table Entry Index 1 Register bits [9:0].

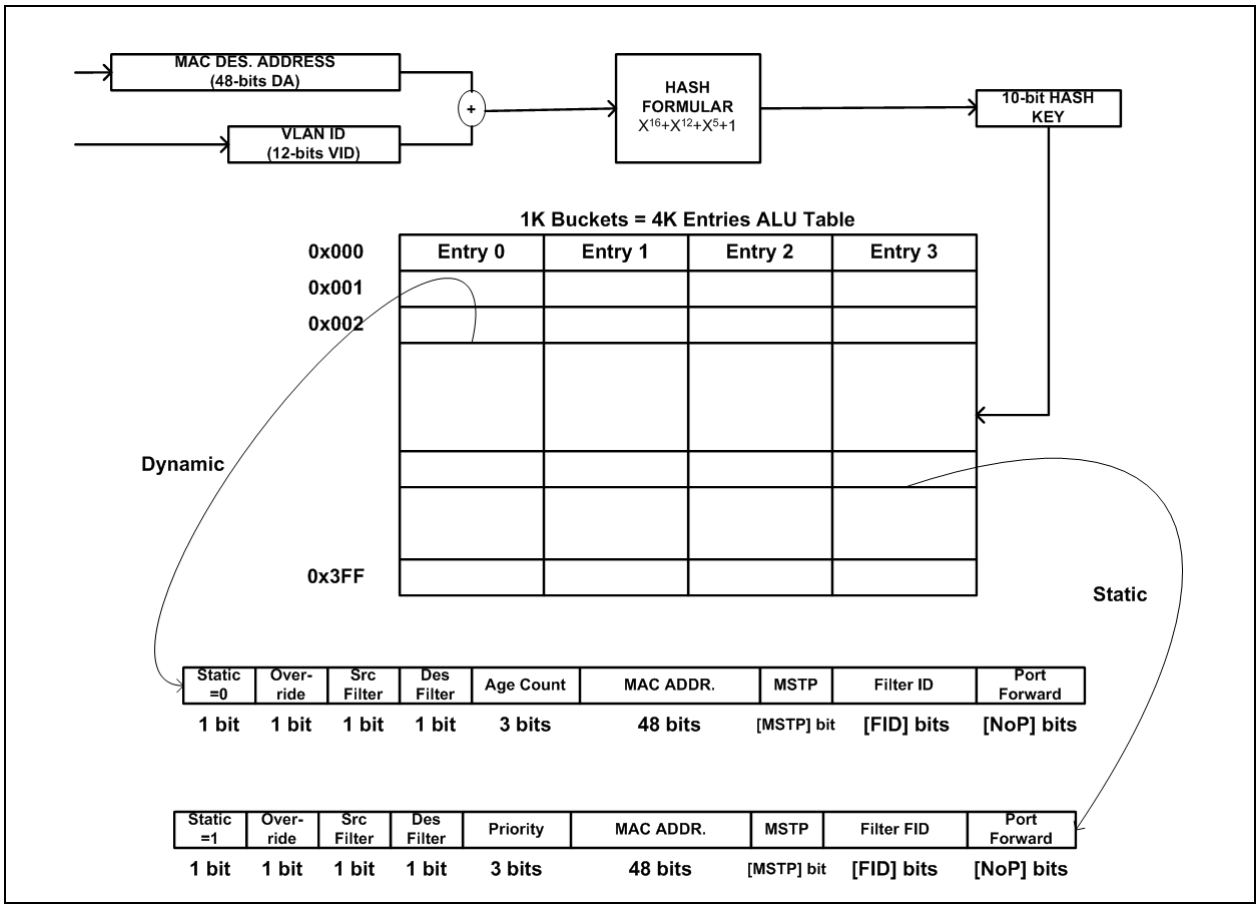
This table is accessed indirectly via the ALU Table registers:

- ALU Table Index 0 Register
- ALU Table Index 1 Register
- ALU Table Access Control Register
- ALU Table Entry 1 Register
- ALU Table Entry 2 Register
- ALU Table Entry 3 Register
- ALU Table Entry 4 Register

All static and dynamic entries may be read, but only static entries may be written. Because most of the table entries are created automatically by hardware address learning, and because the table is 4-way associative, three different methods are available for accessing the memory:

1. Lookup by MAC address. This utilizes the same hash tag lookup circuitry that is used for ingress packet forwarding lookup. The hash tag algorithm is specified by the Hash Option bits in the Switch Lookup Engine Control 0 Register. This is normally how static entries should be written (Read or write).
2. Direct addressing (Read or write).
3. Sequential search, returning all valid entries (Read only).

FIGURE 5-3: ADDRESS LOOKUP TABLE CONFIGURATION



5.3.1.1 Address Lookup Table Read Operation

1. Write the index to the ALU Table Index 0 Register and ALU Table Index 1 Register.
   a) A MAC address is used for the hashing indexing function, which is the normal access mechanism for this table.
   b) A FID is also required if VLAN is enabled.
   c) If directly addressing the table, a 12-bit index is written to bits [11:0] of the MAC address field.
2. Write to the ALU Table Access Control Register.
   a) Set the ACTION field to 10 to indicate a read operation.
   b) Select the addressing method via the DIRECT bit.
   c) Set the START_FINISH bit to initiate the operation.
3. Read / poll the ALU Table Access Control Register.
   a) The START_FINISH bit transitions to 0 to indicate that the operation is complete.
   b) Once START_FINISH is 0, the VALID bit indicates whether or not a valid entry was found. If VALID is false, there is no need to proceed to step 4.
   c) The VALID_ENTRY_OR_SEARCH_END bit is an aggregate of the START_FINISH bit and the VALID bit. It is intended for use when accessing registers by in-band management (IBA), where polling multiple bits is less practical.
4. Read the contents of the returned table entry from the ALU Table Entry 1 Register, ALU Table Entry 2 Register, ALU Table Entry 3 Register, and ALU Table Entry 4 Register. If no VALID entry is returned, these registers will contain all zeros.

5.3.1.2 Address Lookup Table Search Operation

The second method to access the Address Lookup Table is through the search operation. The entire table is searched sequentially, revealing each valid entry. Invalid address entries are skipped, providing an efficient way to search the entire table. Setting the START_FINISH bit in the ALU Table Access Control Register begins the search from the top of the table. This bit is cleared when the search is complete. During the table search, the VALID bit in the ALU Table Access Control Register is cleared when the search starts. The VALID bit indicates when a found valid entry is available in the ALU Table Entry registers (0x0420 - 0x042F). After reading the last ALU Table Entry register (ALU Table Entry 4 Register), the search process automatically continues to seek the next valid entry in the address table. The START_FINISH bit remains set until all the valid entries in the table have been returned. The search can be stopped any time by setting the ALU Table Access Control Register START_FINISH bit to 0.

1. Write to the ALU Table Access Control Register.
   a) Set the ACTION field to 11 to indicate a search operation.
   b) Set the START_FINISH bit to initiate the operation.
2. Poll the VALID bit until it is set.
   a) If register access is by in-band management (IBA) rather than SPI or I^2C, poll VALID_ENTRY_OR_SEARCH_END instead. This bit goes high to indicate either a new valid entry is returned or the search is complete.
3. Read the entry from the ALU Table Entry 1 Register, ALU Table Entry 2 Register, ALU Table Entry 3 Register, and ALU Table Entry 4 Register, in that order.
   a) If the search has ended and there are no more valid entries to read, these registers will return all zeros. In this case, go to step 5.
4. If START_FINISH = 0, go to step 5; else go to step 2.
5. Read VALID_COUNT to verify the number of valid entries.

5.3.1.3 Address Lookup Table Write Operation

1. Perform a read operation to get the contents of the current entry. The values are kept in the ALU Table Entry 1 Register, ALU Table Entry 2 Register, ALU Table Entry 3 Register, and ALU Table Entry 4 Register.
2. Modify the correct entry as necessary. Set the STATIC bit so that the entry is not aged out.
3. Write to the ALU Table Access Control Register.
   a) Set the ACTION field to 01 to indicate a write operation.
   b) Select the addressing method via the DIRECT bit.
   c) Set the START_FINISH bit to initiate the operation.

5.3.1.4 ALU Table Entry 1 Register

Address: 0x0420 - 0x0423 Size: 32 bits

Bits	Description	Type	Default
31	**STATIC** 1 = Entry is static and updated by a host processor; will not be aged out 0 = Entry is dynamically learned and aged	R/W	0b
30	**SRC FILTER** 1 = Drop packet if source address match during source learning 0 = Don't drop if source address match	R/W	0b
29	**DES FILTER** 1 = Drop packet if destination address match during lookup 0 = Don't drop if destination address match	R/W	0b
28:26	**PRIORITY** (for static entries) **AGE COUNT** (for dynamic entries) >0 = Entry has been accessed or learned since last aging process. A default value is reloaded every time the entry is learned or accessed. It is decremented during aging process. 0 = Entry has not been accessed or learned since last aging process. Entry is not valid if it's not static.	R/W	0_00b
25:3	**RESERVED**	RO	0x000000
2:0	**MSTP** Multiple Spanning Tree Protocol group ID for matching	R/W	000b

5.3.1.5 ALU Table Entry 2 Register

Address: 0x0424 - 0x0427 Size: 32 bits

Bits	Description	Type	Default
31	**OVERRIDE** 1 = Enable overriding of port state 0 = Do not enable	R/W	0b
30:7	**RESERVED**	RO	0x000000
6:0	**PORT FORWARD** Each bit corresponds to a device port. Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward to the corresponding port 0 = Do not forward to the corresponding port	R/W	0x00

5.3.1.6 ALU Table Entry 3 Register

Address: 0x0428 - 0x042B Size: 32 bits

Bits	Description	Type	Default
31:23	**RESERVED**	RO	0x000
22:16	**FID** VLAN group ID for matching	R/W	000_0000
15:0	**MAC Address [47:32]**	R/W	0x0000

5.3.1.7 ALU Table Entry 4 Register

Address: 0x042C - 0x042F Size: 32 bits

Bits	Description	Type	Default
31:0	**MAC Address [31:0]**	R/W	0x00000000

5.3.2 STATIC ADDRESS TABLE

The Static Address Table is one of three tables used for MAC address lookup. It can hold up to 16 static address entries, thereby minimizing the number of static entries that may need to be programmed into the Address Lookup Table, which is used primarily for dynamic entries. In response to a destination address (DA) lookup, all tables are searched to make a packet forwarding decision. Entries in this table are programmed by the host processor, and are never aged.

A static DA lookup result (in either this table or the Address Lookup Table) takes precedence over the dynamic DA lookup result.

The Static Address Table has 16 entries and is accessed indirectly. The Static Address and Reserved Multicast Table Control Register is used for indexing and read/write control. The following registers are used for the data fields:

- Static Address Table Entry 1 Register
- Static Address Table Entry 2 Register
- Static Address Table Entry 3 Register
- Static Address Table Entry 4 Register

5.3.2.1 Static Address Table Write Operation

1. Write the content of the table entry to the Static Address Table Entry 1 Register, Static Address Table Entry 2 Register, Static Address Table Entry 3 Register, and Static Address Table Entry 4 Register.
2. Write to the Static Address and Reserved Multicast Table Control Register.
   a) Write the TABLE_INDEX field with the 4-bit index value.
   b) Set the TABLE_SELECT bit to 0 to select the Static Address Table.
   c) Set the ACTION bit to 0 to indicate a write operation.
   d) Set the START_FINISH bit to 1 to initiate the operation.
3. When the operation is complete, the START_FINISH bit will be cleared automatically.

5.3.2.2 Static Address Table Read Operation

1. Write to the Static Address and Reserved Multicast Table Control Register.
   a) Write the TABLE_INDEX field with the 4-bit index value.
   b) Set the TABLE_SELECT bit to 0 to select the Static Address Table.
   c) Set the ACTION bit to 1 to indicate a read operation.

d) Set the START_FINISH bit to 1 to initiate the operation.

2. When the operation is complete, the START_FINISH bit will be cleared automatically.
   a) Read the contents of the indexed entry from the Static Address Table Entry 1 Register, Static Address Table Entry 2 Register, Static Address Table Entry 3 Register, and Static Address Table Entry 4 Register.

5.3.2.3 Static Address Table Entry 1 Register

Address: 0x0420 - 0x0423 Size: 32 bits

Bits	Description	Type	Default
31	**VALID** 1 = Entry is valid 0 = Entry is not valid	R/W	0b
30	**SRC FILTER** 1 = Drop packet if source address match during source learning 0 = Don't drop if source address match	R/W	0b
29	**DES FILTER** 1 = Drop packet if destination address match during lookup 0 = Don't drop if destination address match	R/W	0b
28:26	**PRIORITY**	R/W	0_00b
25:3	**RESERVED**	RO	0x000000
2:0	**MSTP** Multiple Spanning Tree Protocol group ID for matching	R/W	000b

5.3.2.4 Static Address Table Entry 2 Register

Address: 0x0424 - 0x0427 Size: 32 bits

Bits	Description	Type	Default
31	**OVERRIDE** 1 = Enable overriding of port state 0 = Do not enable	R/W	0b
30	**USE FID** Use FID on multicast packets for matching	R/W	0b
29:7	**RESERVED**	RO	0x000000
6:0	**PORT FORWARD** Each bit corresponds to a device port. Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward to the corresponding port 0 = Do not forward to the corresponding port	R/W	0x00

5.3.2.5 Static Address Table Entry 3 Register

Address: 0x0428 - 0x042B Size: 32 bits

Bits	Description	Type	Default
31:23	**RESERVED**	RO	0x000
22:16	**FID** VLAN group ID for matching	R/W	000_0000b
15:0	**MAC Address [47:32]**	R/W	0x0000

5.3.2.6 Static Address Table Entry 4 Register

Address: 0x042C - 0x042F Size: 32 bits

Bits	Description	Type	Default
31:0	**MAC Address [31:0]**	R/W	0x00000000

5.3.3 RESERVED MULTICAST ADDRESS TABLE

The Reserved Multicast Address Table determines the forwarding ports for 48 specific multicast addresses. The table is addressed by the least significant 6 bits of the multicast address, and the table contents are the bits (the PORT_FORWARD field) that represent each possible forwarding port of the device. It is not addressed by the group number in the first column of Table 4-6. Note that the 48 addresses are organized into 8 fixed groups, and changing a forwarding port for one address also makes the same change for all other addresses in the same group.

The Reserved Multicast Table is accessed in the same manner as the Static Address Table, using the same indirect access registers. The Static Address and Reserved Multicast Table Control Register is used for indexing and read/write control, while the Reserved Multicast Address Table Entry 2 Register is used for the data fields.

5.3.3.1 Reserved Multicast Table Write Operation

1. Write the PORT_FORWARD value to the Reserved Multicast Address Table Entry 2 Register.
2. Write to the Static Address and Reserved Multicast Table Control Register.
   a) Write the TABLE_INDEX field with the 6-bit index value.
   b) Set the TABLE_SELECT bit to 1 to select the Reserved Multicast Table.
   c) Set the ACTION bit to 0 to indicate a write operation.
   d) Set the START_FINISH bit to 1 to initiate the operation.
3. When the operation is complete, the START_FINISH bit will be cleared automatically.

5.3.3.2 Reserved Multicast Table Read Operation

1. Write to the Static Address and Reserved Multicast Table Control Register.
   a) Write the TABLE_INDEX field with the 6-bit index value.
   b) Set the TABLE_SELECT bit to 1 to select the Reserved Multicast Table.
   c) Set the ACTION bit to 1 to indicate a read operation.
   d) Set the START_FINISH bit to 1 to initiate the operation.
2. When the operation is complete, the START_FINISH bit will be cleared automatically.
   a) Read the contents of the indexed entry from the Reserved Multicast Address Table Entry 2 Register.

5.3.3.3 Reserved Multicast Address Table Entry 2 Register

Address: 0x0424 - 0x0427 Size: 32 bits

Bits	Description	Type	Default
31:30	**RESERVED**	R/W	00b
29:7	**RESERVED**	RO	0x000000
6:0	**PORT FORWARD** Each bit corresponds to a device port. Bit 0 is for port 1 Bit 1 is for port 2, etc. 1 = Forward to the corresponding port 0 = Do not forward to the corresponding port	R/W	0x00

5.3.4 VLAN TABLE

An internal VLAN Table is used for VLAN lookup. If 802.1Q VLAN mode is enabled (Switch Lookup Engine Control 0 Register), this table will be used to retrieve the VLAN information that is associated with the ingress packet. The table holds 4096 entries - one for each possible VLAN. The table must be set up before 802.1Q VLAN is enabled. The VLAN table is accessed one entry at a time using the following indirect registers:

- VLAN Table Entry 0 Register
- VLAN Table Entry 1 Register
- VLAN Table Entry 2 Register
- VLAN Table Index Register
- VLAN Table Access Control Register

The table data fields are described in Figure 5-4 and Table 5-4.

FIGURE 5-4: VLAN TABLE STRUCTURE

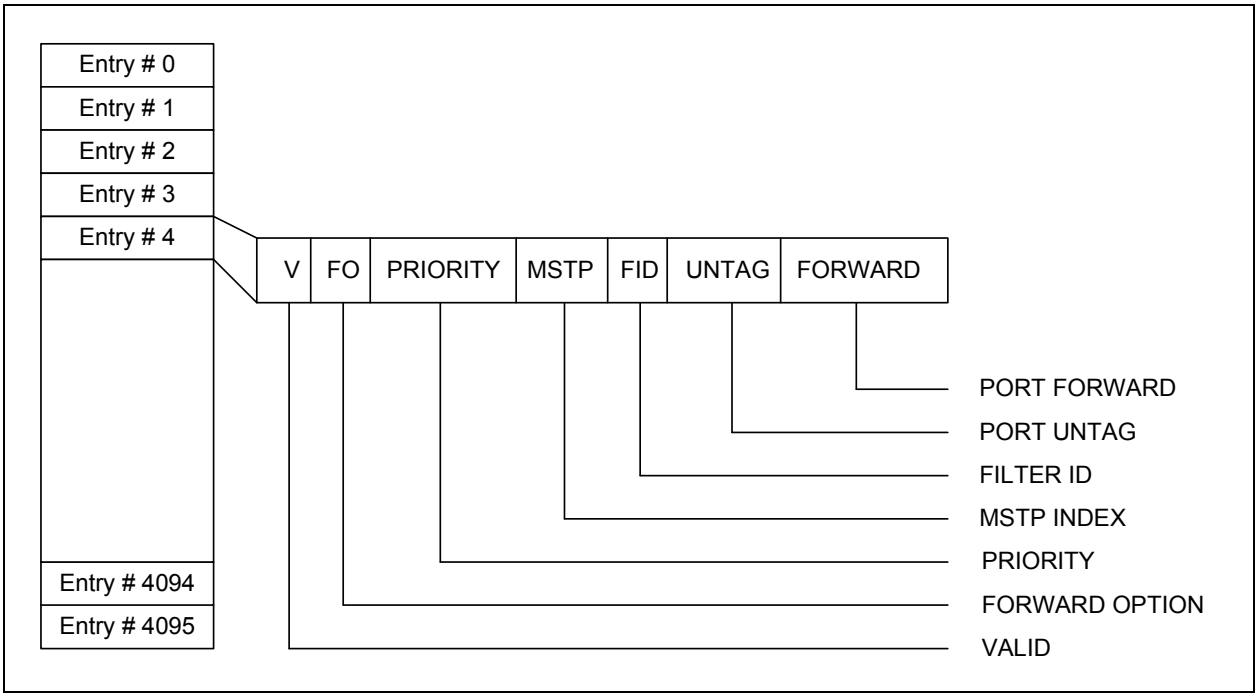


TABLE 5-4: VLAN TABLE DATA FIELDS

Field	Size (bits)	Description
VALID	1	When 1, indicates that the table entry is valid.
FORWARD OPTION	1	When 1, forward to VLAN port table (PORT FORWARD field). When 0, see Table 4-8, "VLAN Forwarding" for details.
PRIORITY	3	Priority value for this VID.
MSTP INDEX	3	Multiple Spanning Tree Protocol index.
FID	7	Filter ID value. It is combined with destination address and hashed to index the Address Lookup Table.
PORT UNTAG	7 (1 per port)	When 1, untag at that egress port. When 0, don't untag.
PORT FORWARD	7 (1 per port)	VLAN port membership list. There is one bit per port, starting with the LSB which corresponds to port 1. A bit value of 1 indicates the associated port is included in the port membership list for that VID. When 0, that port is excluded.

5.3.4.1 VLAN Table Write Operation

1. Write to the VLAN Table Entry 0 Register, VLAN Table Entry 1 Register, and VLAN Table Entry 2 Register to set up the data fields as described in Figure 5-4 and Table 5-4.
2. Write the VLAN Index value in the VLAN Table Index Register. This is the 12-bit index (address) to select the table entry. It is equivalent to the VID which indexes the table during lookup.
3. Write the VLAN Table Access Control Register to specify a write operation, and set START (bit 7). When the operation is complete, bit 7 will be cleared automatically.

5.3.4.2 VLAN Table Read Operation

1. Write the VLAN Index value in the VLAN Table Index Register to select one of the 4k table entries.
2. Write the VLAN Table Access Control Register to specify a read operation and set START (bit 7). When the operation is complete, bit 7 will be cleared automatically.
3. Read the VLAN Table Entry 0 Register, VLAN Table Entry 1 Register, and VLAN Table Entry 2 Register to retrieve the read results from the VLAN table.

5.3.5 ACCESS CONTROL LIST (ACL) TABLE

ACL filtering is implemented individually per-port. The ACL tables are accessed using the Port N: Port Switch ACL Control Registers (0xN600 - 0xN6FF). The 16 entries in each ACL table are addressed indirectly by an index register.

Table 5-5 shows how the various fields of the ACL Table entries are mapped to data registers. The Port ACL Byte Enable MSB Register and Port ACL Byte Enable LSB Register make it possible to write or read any combination of bytes. This is useful for writing the Matching rule, Action rule and Process field separately. There are 16 bits in these byte enable registers, corresponding to the 16 data registers Port ACL Access 0 Register through Port ACL Access F Register. Note that the enable bits are applied in reverse order:

Bit 0 for the Port ACL Access F Register

Bit 1 for the Port ACL Access E Register

…

Bit 14 for the Port ACL Access 1 Register

Bit 15 for the Port ACL Access 0 Register

Also note that the Port ACL Access C Register is not used, so byte enable bit 3 is a don't care.

TABLE 5-5: ACL FIELD REGISTER MAPPING

Register	Bits	MD = 01 ENB = 00 Count Mode	MD = 01 ENB ≠ 00	MD = 10	MD = 11
0xN600	7:4	RESERVED			
	3:0	Process Field: FRN [3:0]			
0xN601	7:6	RESERVED			
	5:4	MD [1:0]			
	3:2	ENB [1:0]			
	1	S / D			
	0	EQ			
0xN602	7:0	MAC ADDRESS [47:0]		IP Address [31:0]	MAX PORT [15:0]
0xN603	7:0				
0xN604	7:0				MIN PORT [15:0]
0xN605	7:0				
0xN606	7:3			IP MASK [31:0]	RESERVED
	2:1				PC [1:0]
	0				PRO [7:0]
0xN607	7:1				
	0				FME
0xN608	7:0	TYPE [15:0]			FMSK [7:0]
0xN609	7:0				FLAG [7:0]
0xN60A	7:6	COUNT [10:3]	Action Rule: PM [1:0]		
	5:3		Action Rule: P [2:0]		
	2		Action Rule: RPE		
	1:0		Action Rule: RP [2:1]		
0xN60B	7	COUNT [2:0]	Action Field: RP [0]		
	6:5		Action Field: MM [1:0]		
	4:0	RESERVED			
0xN60C	7:0	RESERVED			
0xN60D	7	RESERVED			
	6	TU	Action Field: FORWARD [6:0]		
	5	CA			
	4:0	RESERVED			
0xN60E	7:0		Process Field: RuleSet [15:8]		
0xN60F	7:0		Process Field: RuleSet [7:0]		

5.3.5.1 ACL Table Read

1. Write to the Port ACL Access Control 0 Register with the table entry number (0 to 15) in the ACL Index field, and the Write/Read bit 4 cleared to zero. This one write to this register initiates the read operation.
2. Poll the Read Status bit in the Port ACL Access Control 0 Register to determine when the read operation is complete.
3. When the operation is complete, data may be retrieved from the Port ACL Access 0 Register through Port ACL Access F Register.

5.3.5.2 ACL Table Write

1. Write the ACL table entry values to the Port ACL Access 0 Register through Port ACL Access F Register.
2. Write the Port ACL Byte Enable MSB Register and Port ACL Byte Enable LSB Register to select which registers (Port ACL Access 0 Register through Port ACL Access F Register) are to be written into the ACL table.
3. Write to the Port ACL Access Control 0 Register with the table entry number in the ACL Index field, and the Write/Read bit 4 set to one. This one write to this register initiates the write operation.
4. The Write Status bit in the Port ACL Access Control 0 Register may be polled to determine when the operation is complete.

5.3.6 MANAGEMENT INFORMATION BASE (MIB) COUNTERS

There are 36 MIB counters per port. These counters accumulate a variety of statistics on ingress and egress traffic and events for network management. They are accessed indirectly using the Port MIB Control and Status Register and Port MIB Data Register. The Switch MIB Control Register provides global flush and freeze control of the MIB counters.

TABLE 5-6: MIB COUNTERS

MIB Index	MIB Counter	Size (bits)	Description
0x00	RxHiPriorityByte	30	RX high priority octet count, including bad packets.
0x01	RxUndersizePkt	30	RX undersize packets with good CRC.
0x02	RxFragments	30	RX fragment packets with bad CRC, symbol errors or alignment errors.
0x03	RxOversize	30	RX oversize packets w/ good CRC (max: 1536 or 1522 bytes).
0x04	RxJabbers	30	RX packets longer than 1522 bytes with either CRC errors, alignment errors or symbol errors (depends on max packet size setting); or RX packets longer than 1916 bytes only.
0x05	RxSymbolError	30	RX packets with invalid data symbol; and legal preamble and packet size.
0x06	RxCRCerror	30	RX packets between 64 and 1522 bytes in size, with an integral number of bytes and a bad CRC. (Upper limit depends on max packet size setting.)
0x07	RxAlighmentError	30	RX packets between 64 and 1522 bytes in size, with a non-integral number of bytes and a bad CRC. (Upper limit depends on max packet size setting.)
0x08	RxControl8808Pkts	30	MAC control frames received with 0x8808 in the EtherType field.
0x09	RxPausePkts	30	PAUSE frames received. PAUSE is defined as EtherType (0x8808), DA, control opcode (0x0001), minimum 64 byte data length, and a valid CRC.
0x0A	RxBroadcast	30	RX good broadcast packets. Does not include erred broadcast packets or valid multicast packets.
0x0B	RXMulticast	30	RX good multicast packets. Does not include MAC control frames, erred multicast packets, or valid broadcast packets.
0x0C	RxUnicast	30	RX good unicast packets.
0x0D	Rx64Octets	30	RX packets (bad packets included) that are 64 bytes in length.
0x0E	Rx65to127Octets	30	RX packets (bad packets included) that are 65 to 127 bytes in length.
0x0F	Rx128to255Octets	30	RX packets (bad packets included) that are 128 to 255 bytes in length.
0x10	Rx256to511Octets	30	RX packets (bad packets included) that are 256 to 511 bytes in length.
0x11	Rx512to2023Octets	30	RX packets (bad packets included) that are 512 to 1023 bytes in length.
0x12	Rx1024to1522Octets	30	RX packets (bad packets included) that are 1024 to 1522 bytes in length.
0x13	Rx1523to2000Octets	30	RX packets (bad packets included) that are 1523 t0 2000 bytes in length.
0x14	Rx2001+Octets	30	RX packets (bad packets included) that are between 2001 bytes and the upper limit in length.

TABLE 5-6: MIB COUNTERS (CONTINUED)

MIB Index	MIB Counter	Size (bits)	Description
0x15	TxHiPriorityByte	30	TX high priority good octet count, including PAUSE packets.
0x16	TxLateCollision	30	Collision is detected later than 512 bit times into the transmission of a packet.
0x17	TxPausePkts	30	PAUSE frames transmitted. PAUSE is EtherType (0x8808), DA, control opcode (0x0001), minimum 64 byte data length, and a valid CRC.
0x18	TxBroadcastPkts	30	TX good broadcast packets. Does not include erred broadcast packets or valid multicast packets.
0x19	TxMulticastPkts	30	TX good multicast packets. Does not include MAC control frames, erred multicast packets, or valid broadcast packets.
0x1A	TxUnicastPkts	30	TX good unicast packets.
0x1B	TxDeferred	30	TX packets where the first transmit attempt is delayed due to the busy medium.
0x1C	TxTotalCollision	30	TX total collisions. Half duplex only.
0x1D	TxExcessiveCollision	30	TX fails due to excessive collisions.
0x1E	TxSingleCollision	30	Successfully transmitted frames where transmission is inhibited by exactly one collision.
0x1F	TxMultipleCollision	30	Successfully transmitted frames where transmission is inhibited by more than one collision.
0x80	RxByteCnt	36	RX byte count.
0x81	TxByteCnt	36	TX byte count.
0x82	RxDropPackets	30	RX packets dropped due to lack of resources.
0x83	TXDropPackets	30	TX packets dropped due to lack of resources.

5.3.6.1 MIB Counter Read Operation

Indirect access registers are used to read the MIB counters. Separate access registers are provided for each port via the Port MIB Control and Status Register and Port MIB Data Register. All MIB Counters are read-clear. The steps for reading a counter are as follows:

1. Write the MIB Index to bits [23:16] of the Port MIB Control and Status Register.
2. Set the MIB Read Enable in bit 25 of the Port MIB Control and Status Register. This step and the previous step may be done together.
3. Read the MIB Read Enable / Count Valid in bit 25 of the Port MIB Control and Status Register. A '0' value indicates that the read is complete and the count is valid.
4. Read the count value from the Port MIB Data Register. For 36-bit counters, counter bits [35:32] are read from the Port MIB Control and Status Register. The Counter Overflow bit is also found in the Port MIB Control and Status Register.

5.3.6.2 MIB Counter Freeze and Flush Functions

Counter freeze and flush functions are available on a port-by-port basis. Freezing or flushing counters is initiated by setting the appropriate bit in the Switch MIB Control Register. The freeze or flush function will be applied to all ports for which the flush and freeze functions have been enabled. To enable flush and freeze for a port, set bit 24 in the Port MIB Control and Status Register.

The following steps show an example of how flush and freeze are used to collect MIB statistics for all ports for a period of 1 second:

1. Set the MIB Flush and Freeze Enable bit 24 in the Port MIB Control and Status Register for all ports N.
2. Write 0x40 to the Switch MIB Control Register to freeze the MIB counters for all enabled ports.
3. Write 0xC0 to the Switch MIB Control Register to clear the MIB counters for all enabled ports (while continuing to also freeze the counters).
4. At the beginning of the 1 second period, write 0x00 to the Switch MIB Control Register to enable the counters.
5. At the end of the 1 second period, write 0x40 to the Switch MIB Control Register to freeze the counters.
6. Read each counter for each port.

5.4 MDIO Manageable Device (MMD) Registers (Indirect)

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. However, the KSZ8567R uses only a small fraction of the available registers. Refer to Table 5-7, "MMD Register Map" for a list of accessible MMD device addresses and their associated register addresses. Detailed descriptions of the supported MMD registers are provided in the following subsections.

The following two standard port registers serve as the portal registers to access the indirect MMD registers.

- PHY MMD Setup Register
- PHY MMD Data Register

TABLE 5-7: MMD REGISTER MAP

Device Address (hex)	Register Address (hex)	Description
2h	00h	MMD LED Mode Register
7h	3Ch	MMD EEE Advertisement Register

Example: MMD Register Write

Write MMD - Device Address 2h, Register 00h = 0010h to enable single-LED mode.

1. Write the PHY MMD Setup Register with 0002h // Set up register address for MMD – Device Address 2h.
2. Write the PHY MMD Data Register with 0000h // Select Register 00h of MMD – Device Address 2h.
3. Write the PHY MMD Setup Register with 4002h // Select register data for MMD – Device Address 2h, Reg. 00h.
4. Write the PHY MMD Data Register with 0010h // Write value 0010h to MMD – Device Address 2h, Reg. 00h.

Example: MMD Register Read

Read MMD - Device Address 2h, Register 11h – 13h for the LED mode status.

1. Write the PHY MMD Setup Register with 0002h // Set up register address for MMD – Device Address 2h.
2. Write the PHY MMD Data Register with 0000h // Select Register 00h of MMD – Device Address 2h.
3. Write the PHY MMD Setup Register with 4002h // Select register data for MMD – Device Address 2h, Reg. 00h.
4. Read the PHY MMD Data Register // Read data in MMD – Device Address 2h, Reg. 00h.

5.4.1 MMD LED MODE REGISTER

MMD Address: 0x02 Size: 16 bits
Register: 0x00

Bits	Description	Type	Default
15:5	**RESERVED**	RO	0x000
4	**LED Mode** 1 = Single-LED Mode 0 = Tri-color Dual-LED Mode	R/W	0b
3:0	**RESERVED**	RO	0001b

5.4.2 MMD EEE ADVERTISEMENT REGISTER

MMD Address: 0x07 Size: 16 bits
Register: 0x3C

Bits	Description	Type	Default
15:2	**RESERVED**	RO	0x000
1	**100BASE-T EEE Enable** 1 = 100 Mbps EEE capable 0 = No 100 Mbps EEE capability	R/W	1b
0	**RESERVED**	RO	0b

6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (**AVDDL**, **DVDDL**) . . . . . -0.5 V to +1.8 V
Supply Voltage (**AVDDH**, **VDDIO**) . . . . . -0.5 V to +5.0 V
Input Voltage (all inputs) . . . . . -0.5 V to +5.0 V
Output Voltage (all outputs) . . . . . -0.5 V to +5.0 V
Lead Temperature (soldering, 20 sec.) . . . . . +260°C
Storage Temperature (T_S) . . . . . -65°C to +150°C
Maximum Junction Temperature (T_J) . . . . . +125°C
HBM ESD Performance . . . . . +/-6 kV

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 6.2, "Operating Conditions**", Section 6.3, "Electrical Characteristics", or any other applicable section of this specification is not implied.

6.2 Operating Conditions**

Supply Voltage (**AVDDL**, **DVDDL**) . . . . . +1.14V to +1.26 V
Supply Voltage (**AVDDH** @ 3.3V) . . . . . +3.135 V to +3.465 V
Supply Voltage (**AVDDH** @ 2.5V) . . . . . +2.375 V to +2.625 V
Supply Voltage (**VDDIO** @ 3.3V) . . . . . +3.135 V to +3.465 V
Supply Voltage (**VDDIO** @ 2.5V) . . . . . +2.375 V to +2.625 V
Supply Voltage (**VDDIO** @ 1.8V) . . . . . +1.71 V to +1.89 V
Ambient Operating Temperature in Still Air (T_A) . . . . . Note 6-1
Junction to Ambient Resistance (Θ_{JA}) (Note 6-2) . . . . . Note 6-3
Junction to Case Characterization (Ψ_{JT}) (Note 6-2) . . . . . 0.04°C/W
Junction to Case Resistance (Θ_{JC}) (Note 6-2) . . . . . Note 6-4

Note 6-1 -40°C to +105°C for extended version, -40°C to +85°C for industrial version.

Note 6-2 Ψ_{JT} and Θ_{JA} are under a 0 m/s air velocity. A 6-layer PCB is required for industrial applications.

Note 6-3 11.3°C/W on a 6-layer PCB per JESD51, 14.4°C/W on a 4-layer PCB per JESD51.

Note 6-4 1.5°C/W on a 6-layer PCB per JESD51, 1.21°C/W on a 4-layer PCB per JESD51.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

6.3 Electrical Characteristics

T_A = 25°C.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current - Mixed 1000/100 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**AVDDH** @ 2.5V; **VDDIO** @ 3.3V Ports 1-5 in 100BASE-TX Ports 6 & 7 in RGMII (1000 Mbps) All ports 100% utilization		150		mA
I_{DD_IO}	**VDDIO** supply current			80		mA
I_{DD_CA}	**AVDDL** supply current			140		mA
I_{DD_CD}	**DVDDL** supply current			350		mA
Supply Current - Full 100 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**AVDDH** @ 2.5V; **VDDIO** @ 3.3V Ports 1-5 in 100BASE-TX Ports 6 & 7 in MII (100 Mbps) All ports 100% utilization		140		mA
I_{DD_IO}	**VDDIO** supply current			35		mA
I_{DD_CA}	**AVDDL** supply current			140		mA
I_{DD_CD}	**DVDDL** supply current			350		mA
Supply Current - Full 10 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**AVDDH** @ 2.5V; **VDDIO** @ 3.3V Ports 1-5 in 10BASE-Te Ports 6 & 7 in MII (10 Mbps) All ports 100% utilization		100		mA
I_{DD_IO}	**VDDIO** supply current (3.3V)			30		mA
I_{DD_CA}	**AVDDL** supply current			30		mA
I_{DD_CD}	**DVDDL** supply current			150		mA
Supply Current - Power Management - Energy Detect Mode						
I_{DD_AH}	**AVDDH** supply current			20		mA
I_{DD_IO}	**VDDIO** supply current (3.3V)			30		mA
I_{DD_CA}	**AVDDL** supply current			30		mA
I_{DD_CD}	**DVDDL** supply current			150		mA
Supply Current - Power Management - Global Soft Power Down Mode						
I_{DD_AH}	**AVDDH** supply current			2		mA
I_{DD_IO}	**VDDIO** supply current (3.3V)			6		mA
I_{DD_CA}	**AVDDL** supply current			0.01		mA
I_{DD_CD}	**DVDDL** supply current			5		mA
I Type CMOS Input Buffers (VDDIO = 3.3/2.5/1.8V)						
V_{IH}	Input High Voltage		2.1/1.7/1.3			V
V_{IL}	Input Low Voltage				0.9/0.9/0.6	V
I_{IN}	Input Current	V_{IN} = **GND ~ VDDIO**	-10		10	µA
O8 Type CMOS Output Buffers (VDDIO = 3.3/2.5/1.8V)						
V_{OH}	Output High Voltage	I_{OH} = 8/8/6 mA	2.4/1.9/1.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8/8/6 mA			0.4/0.4/0.2	V
I_{OZ}	Output Tri-State Leakage	V_{IN} = **GND ~ VDDIO**			10	µA

TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
O24 Type CMOS Output Buffers (VDDIO = 3.3/2.5/1.8V)						
V_{OH}	Output High Voltage	I_{OH} = 24/24/20 mA	2.4/1.9/1.5			V
V_{OL}	Output Low Voltage	I_{OL} = 24/24/20 mA			0.4/0.4/0.2	V
I_{OZ}	Output Tri-State Leakage	V_{IN} = GND ~ VDDIO			10	µA
I/O Pin Internal Pull-Up and Pull-Down Effective Resistance						
R1.8PU	I/O Pin Effective Pull-Up Resistance	VDDIO = 1.8V		125		kΩ
R1.8PD	I/O Pin Effective Pull-Down Resistance			97		kΩ
R2.5PU	I/O Pin Effective Pull-Up Resistance	VDDIO = 2.5V		58		kΩ
R2.5PD	I/O Pin Effective Pull-Down Resistance			51		kΩ
R3.3PU	I/O Pin Effective Pull-Up Resistance	VDDIO = 3.3V		38		kΩ
R3.3PD	I/O Pin Effective Pull-Down Resistance			39		kΩ
100BASE-TX Transmit (Measured Differentially After 1:1 Transformer)						
V_O	Peak Differential Output	100Ω termination on the differential output	±0.95		±1.05	V
V_{imb}	Output Voltage Imbalance	100Ω termination on the differential output			2	%
t_r , t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty cycle Distortion				±0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET (using 6.04kΩ - 1% resistor)			1.21		V
	Output Jitter	Peak-to-Peak		0.7	1.4	ns
10BASE-T/Te Receive						
V_{sq}	Squelch Threshold	5MHz Square Wave		400		mV
10BASE-Te Transmit (Measured Differentially After 1:1 Transformer)						
V_p	Peak Differential Output Voltage	100Ω termination on the differential output	1.54	1.75	1.96	V
	Jitter Added	100Ω termination on the differential output (peak-to-peak)			3.5	ns
t_r , t_f	Rise/Fall Time			25		ns

TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
10BASE-T Transmit (Measured Differentially After 1:1 Transformer)						
V_p	Peak Differential Output Voltage	100Ω termination on the differential output	2.2	2.5	2.8	V
	Jitter Added	100Ω termination on the differential output (peak-to-peak)			3.5	ns
t_r , t_f	Rise/Fall Time			25		ns

6.4 Timing Specifications

This section details the various timing specifications of the device.

Note: The I^2C interface timing adheres to the NXP *I^2C-Bus Specification* (UM10204, Rev. 6) (high-speed mode and slower). Refer to the *I^2C-Bus Specification* for additional information.

6.4.1 RGMII TIMING

Figure 6-1 illustrates the RGMII timing requirements.

FIGURE 6-1: RGMII TIMING

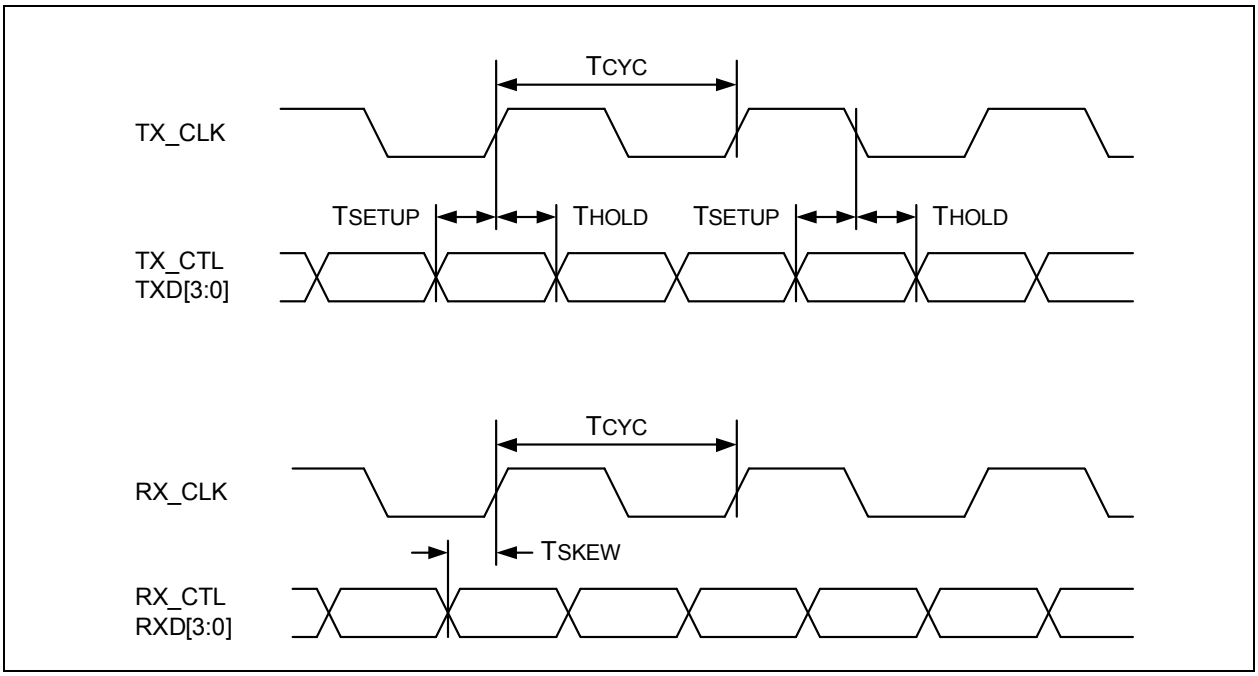


TABLE 6-2: RGMII TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
T_{SETUP}	Port 6 Data to clock input setup (Note 6-5)	2.2			ns
	Port 7 Data to clock input setup (Note 6-5)	1.3			ns
T_{HOLD}	Port 6 Data to clock input hold (Note 6-5)	0			ns
	Port 7 Data to clock input hold (Note 6-5)	0.7			ns
T_{SKEW}	Data to clock output skew (Note 6-6)	1.2	2.0		ns
T_{CYC}	Clock cycle duration (Note 6-7)	7.2	8	8.8	ns
Duty_G	1000Mbps duty cycle	45	50	55	%
Duty_T	10/100Mbps duty cycle	40	50	60	%
T_r / T_f	Rise / Fall time (20-80%)			Note 6-8	ns

Note 6-5 For cases where there is no (or insufficient) skew between the input data and input clock, it is possible to add internal delay to the TX_CLK pinout by setting the RGMII Ingress Internal Delay bit in the XMII Port Control 1 Register register. This feature reduces the setup time requirement and increases the hold time requirement nominally by 1.3ns.

Note 6-6 The RGMII interface adheres to the RGMII Specification Version 2.0, which specified that the driving device delay the output clock relative to the output data. This is the T_{SKEW} parameter. This skew can be disabled by clearing the RGMII Egress Internal Delay bit in the XMII Port Control 1 Register register. Generally this is not recommended.

Note 6-7 For 10Mbps and 100Mbps, T_{CYC} will scale to 400ns +/- 40ns and 40ns +/- 4 ns, respectively.

Note 6-8 0.75ns for **VDDIO** = 3.3V/2.5V, 1.0ns for **VDDIO** = 1.8V

6.4.2 MII TIMING

6.4.2.1 MII Transmit Timing in MAC Mode

Figure 6-2 illustrates a write operation from the KSZ8567R to a PHY or other device while operating the KSZ8567R in MAC Mode.

FIGURE 6-2: MII TRANSMIT TIMING IN MAC MODE

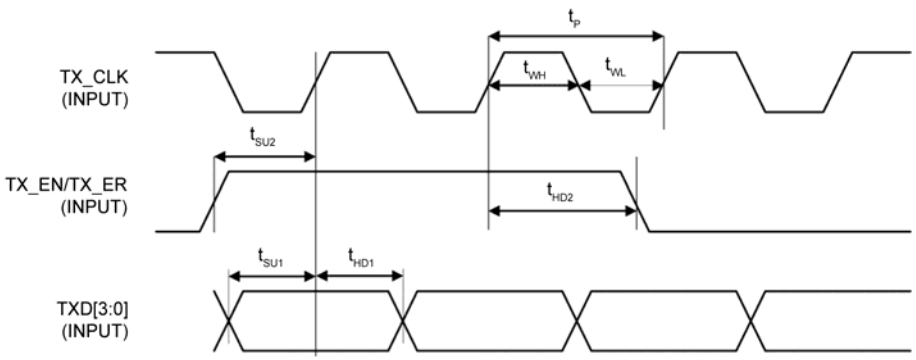


TABLE 6-3: MII TRANSMIT TIMING IN MAC MODE VALUES

Symbol	Description	Min	Typ	Max	Units
t_P (100BASE-TX/ 10BASE-T/Te)	**RX_CLK** period		40/400		ns
t_{WL} (100BASE-TX/ 10BASE-T/Te)	**RX_CLK** pulse width low		20/200		ns
t_{WH} (100BASE-TX/ 10BASE-T/Te)	**RX_CLK** pulse width high		20/200		ns
t_{OD}	**RX_DV**, **RXD_[3:0]** output delay from rising edge of **RX_CLK**		16		ns

6.4.2.2 MII Receive Timing in MAC Mode

Figure 6-3 illustrates a read operation by the KSZ8567R from a PHY or other device while operating the KSZ8567R in MAC Mode.

FIGURE 6-3: MII RECEIVE TIMING IN MAC MODE

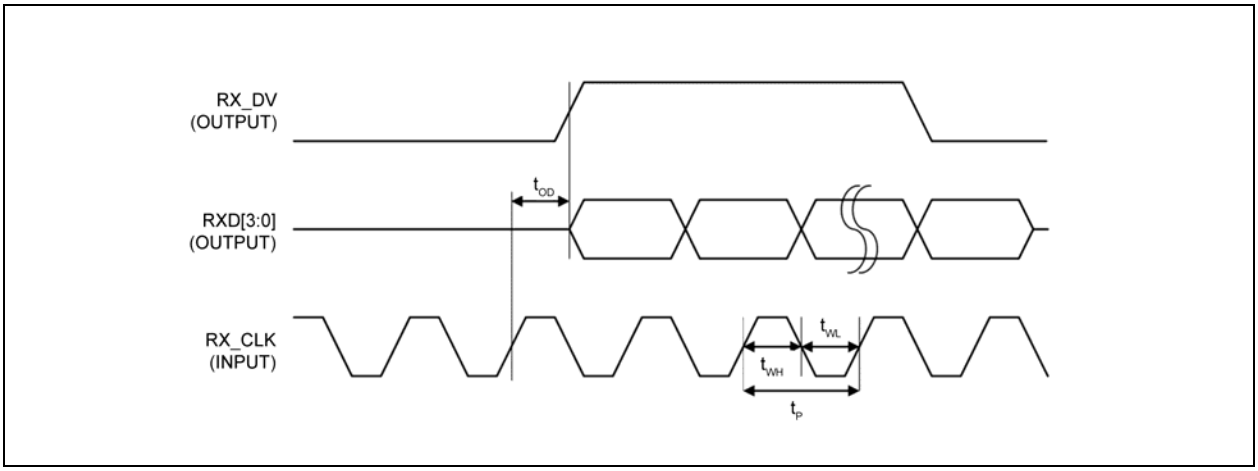


TABLE 6-4: MII RECEIVE TIMING IN MAC MODE VALUES

Symbol	Description	Min	Typ	Max	Units
t_P (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** period		40/400		ns
t_{WL} (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** pulse width low		20/200		ns
t_{WH} (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** pulse width high		20/200		ns
t_{SU1}	**TXD_[3:0]** setup time to rising edge of **TX_CLK**	10			ns
t_{SU2}	**TX_EN**, **TX_ER** setup time to rising edge of **TX_CLK**	10			ns
t_{HD1}	**TXD_[3:0]** hold time from rising edge of **TX_CLK**	10			ns
t_{HD2}	**TX_EN**, **TX_ER** hold time from rising edge of **TX_CLK**	10			ns

6.4.2.3 MII Receive Timing in PHY Mode

FIGURE 6-4: MII RECEIVE TIMING IN PHY MODE

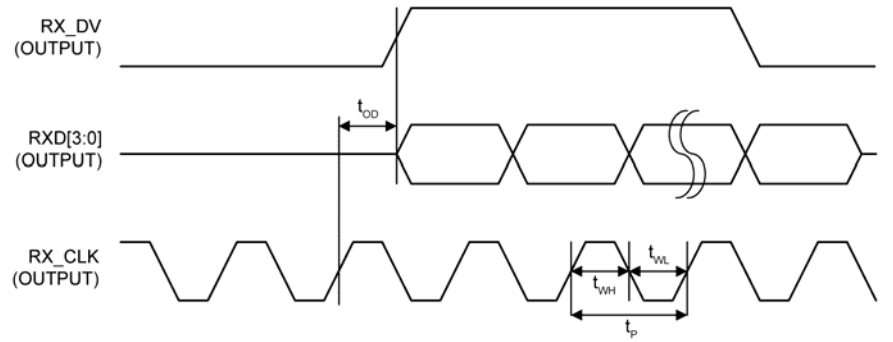


TABLE 6-5: MII RECEIVE TIMING IN PHY MODE VALUES

Symbol	Description	Min	Typ	Max	Units
t_P (100BASE-TX / 10BASE-T/Te)	**RX_CLK** period		40/400		ns
t_{WL} (100BASE-TX / 10BASE-T/Te)	**RX_CLK** pulse width low		20/200		ns
t_{WH} (100BASE-TX / 10BASE-T/Te)	**RX_CLK** pulse width high		20/200		ns
t_{OD}	**RX_DV**, **RXD_[3:0]** output delay from rising edge of **RX_CLK**		20		ns

6.4.2.4 MII Transmit Timing in PHY Mode

FIGURE 6-5: MII TRANSMIT TIMING IN PHY MODE

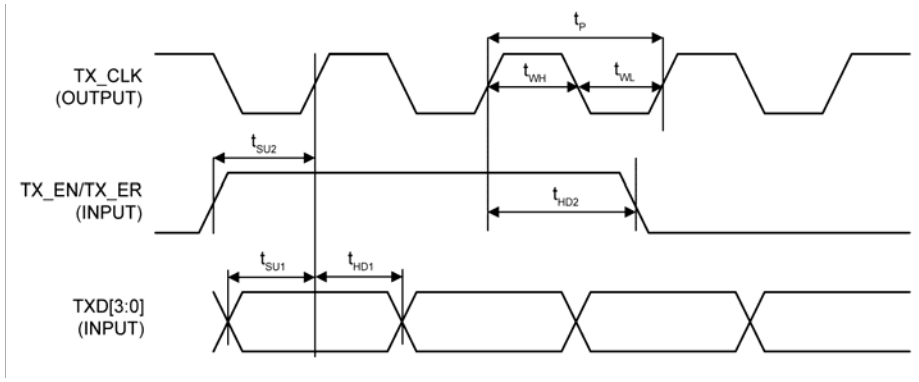


TABLE 6-6: MII TRANSMIT TIMING IN PHY MODE VALUES

Symbol	Description	Min	Typ	Max	Units
t_P (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** period		40/400		ns
t_{WL} (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** pulse width low		20/200		ns
t_{WH} (100BASE-TX/ 10BASE-T/Te)	**TX_CLK** pulse width high		20/200		ns
t_{SU1}	**TXD_[3:0]** setup time to rising edge of **TX_CLK**	10			ns
t_{SU2}	**TX_EN**, **TX_ER** setup time to rising edge of **TX_CLK**	10			ns
t_{HD1}	**TXD_[3:0]** hold time from rising edge of **TX_CLK**	0			ns
t_{HD2}	**TX_EN**, **TX_ER** hold time from rising edge of **TX_CLK**	0			ns

6.4.3 RMII TIMING

Figure 6-6 and Figure 6-7 illustrate the RMII timing requirements.

FIGURE 6-6: RMII TRANSMIT TIMING

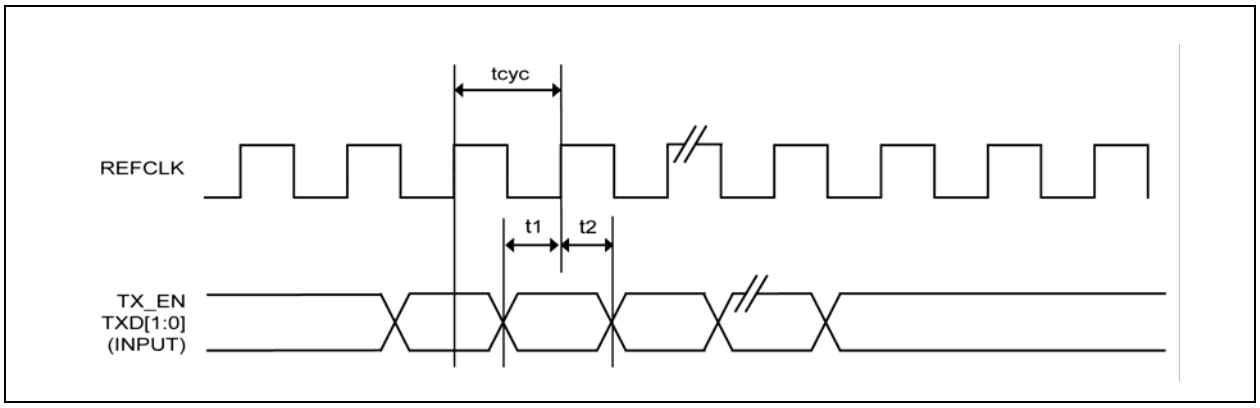


FIGURE 6-7: RMII RECEIVE TIMING

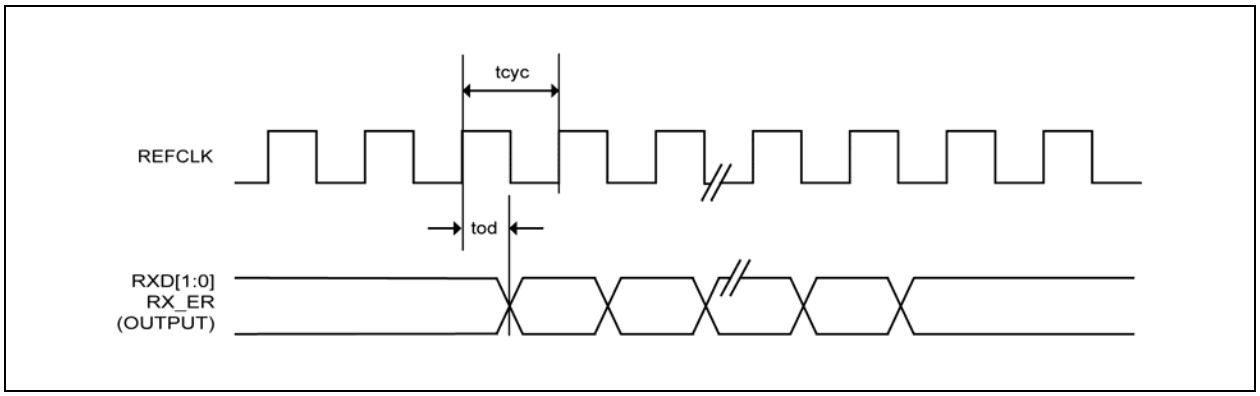


TABLE 6-7: RMII TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{od}	Output delay	7	9	13	ns

6.4.4 MIIM TIMING

Figure 6-8 illustrates the MIIM timing requirements.

FIGURE 6-8: MIIM TIMING

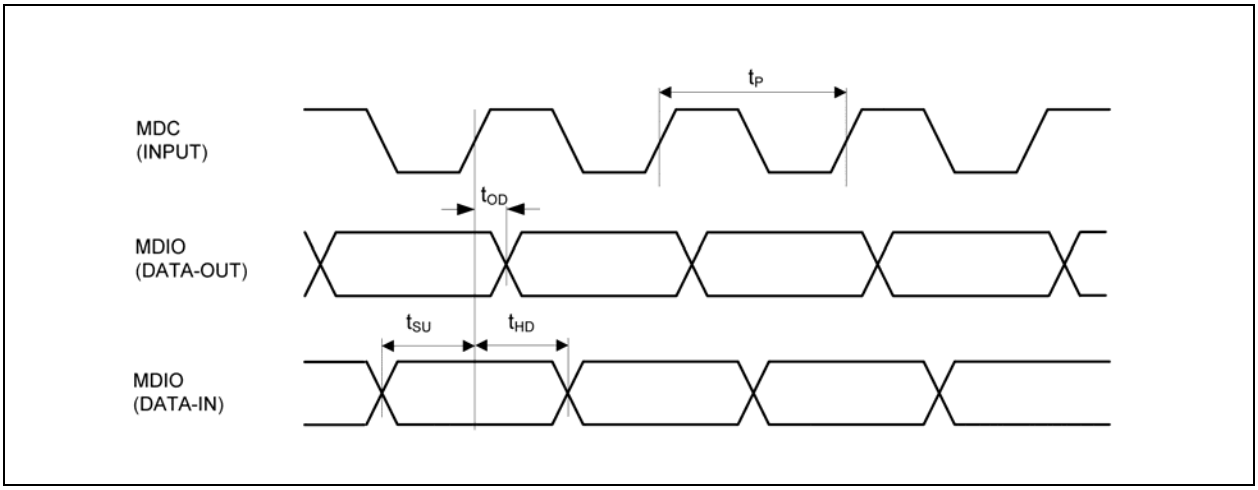


TABLE 6-8: MIIM TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_P	**MDC** period		400		ns
t_{OD}	Output delay		200		ns
t_{SU}	**MDIO** setup time to rising edge of **MDC**	10			ns
t_{HD}	**MDIO** hold time from rising edge of **MDC**	5			ns

6.4.5 SPI TIMING

Figure 6-9 and Figure 6-10 illustrate the SPI timing requirements.

FIGURE 6-9: SPI DATA INPUT TIMING

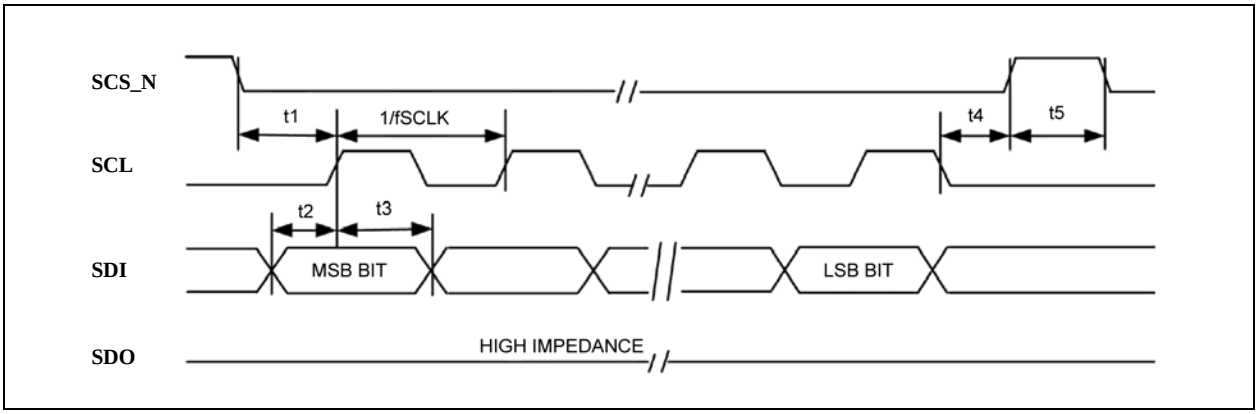


FIGURE 6-10: SPI DATA OUTPUT TIMING

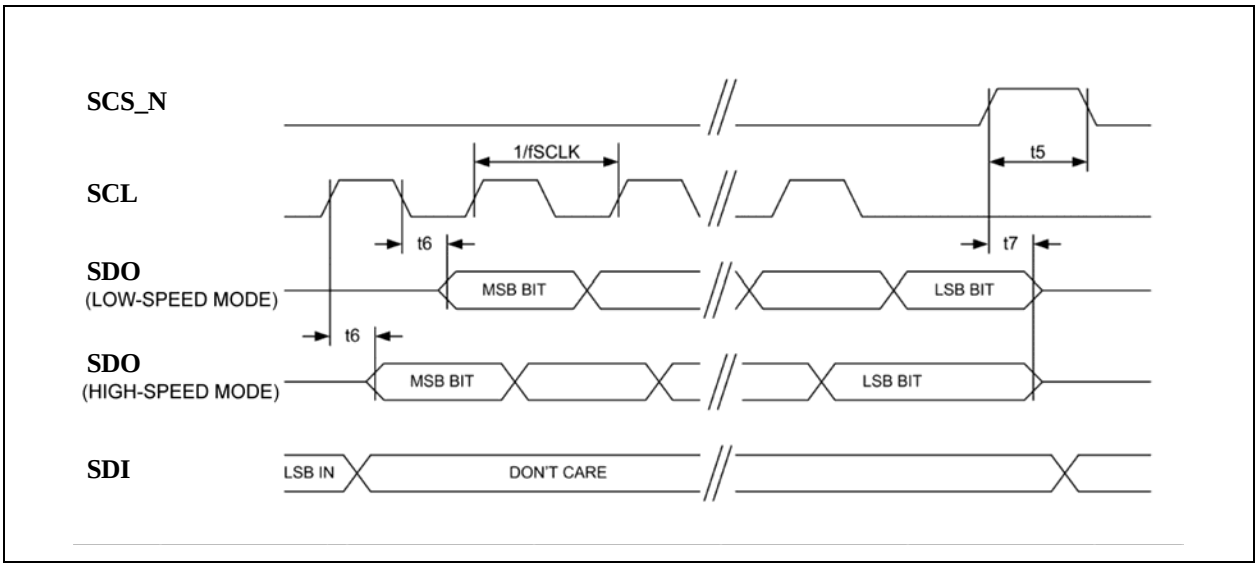


TABLE 6-9: SPI TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
f_{SCLK}	**SCL** clock frequency			50	MHz
t_1	**SCS_N** active setup time	8			ns
t_2	**SDI** data input setup time	3			ns
t_3	**SDI** data input hold time	3			ns
t_4	**SCS_N** active hold time	8			ns
t_5	**SCS_N** disable high time	8			ns
t_6	**SCL** falling edge to **SDO** data output valid	2		9	ns
t_7	**SCS_N** inactive to **SDO** data input invalid	1			ns

6.4.6 AUTO-NEGOTIATION TIMING

Figure 6-11 illustrates the Auto-Negotiation timing requirements.

FIGURE 6-11: AUTO-NEGOTIATION TIMING

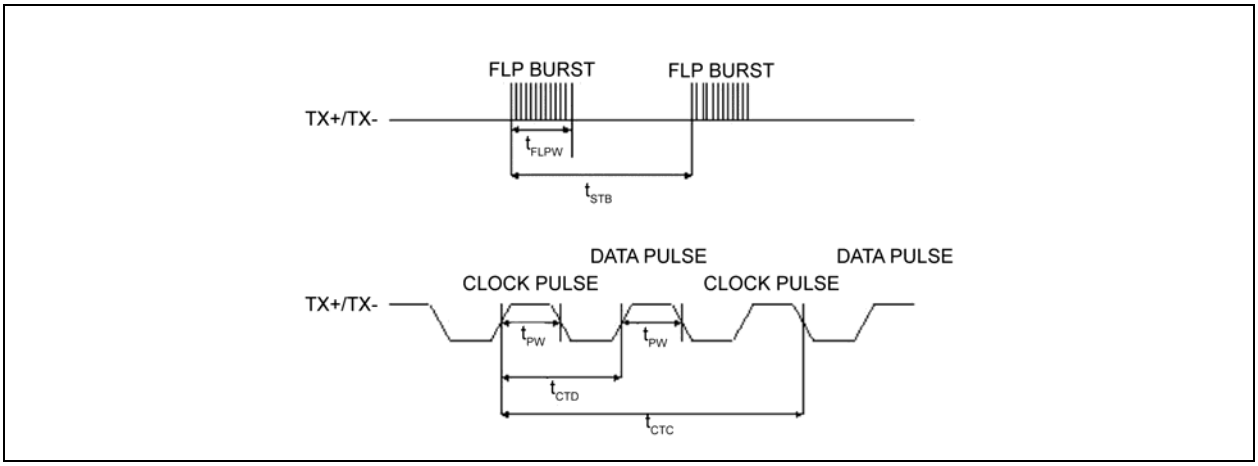


TABLE 6-10: AUTO-NEGOTIATION TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per burst	17		33	

6.4.7 TRIGGER OUTPUT UNIT AND TIMESTAMP INPUT UNIT TIMING

Figure 6-12 provides details and constraints on various timing relationships within the twelve trigger output units and the timestamp input units.

FIGURE 6-12: TRIGGER OUTPUT UNIT AND TIMESTAMP INPUT UNIT TIMING

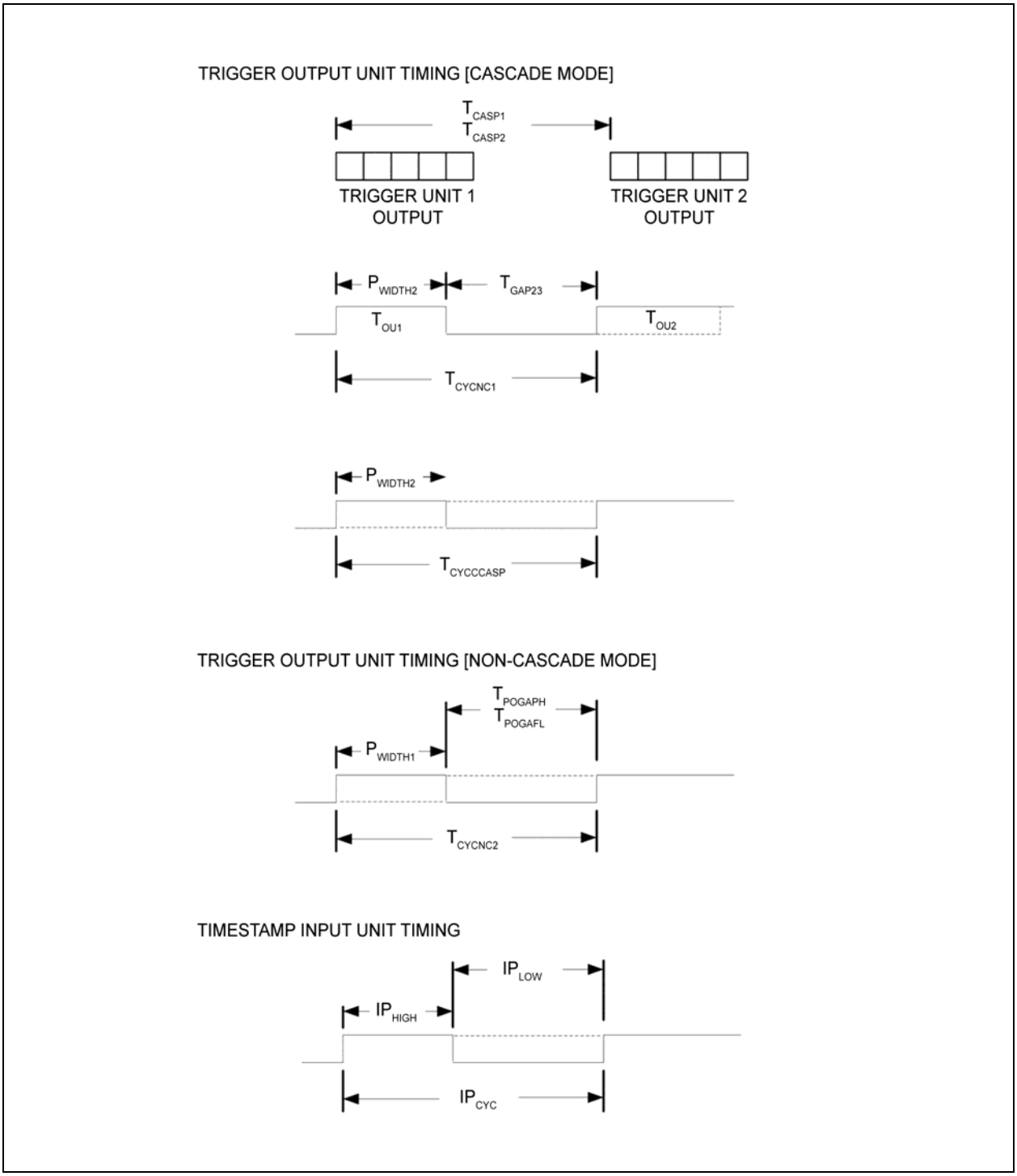


TABLE 6-11: AUTO-NEGOTIATION TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
Trigger Output Unit Timing (Cascade Mode)					
t_{CASP1}	In cascade mode for TRIGX_CFG_1[6:4] = 100, or 101, or 110 (Neg. Edge, Pos. Edge, and Shift Reg. Output signals). Minimum time between start of one TOU and the start of another TOU cascaded on the same GPIO pin.	80			ns
t_{CASP2}	In cascade mode for TRIGX_CFG_1[6:4] = 010, 011, 100, or 101 (Neg. Pulse, Pos. Pulse, Neg. Periodic, and Pos. Periodic Output signals). Minimum time between start of one TOU and the start of another TOU cascaded on the same GPIO pin.	120			ns
$t_{CYCCASP}$	In cascade mode for TRIGX_CFG_1[6:4] = 010, and 011 (Neg. Pulse, Pos. Pulse Output signals). In cascade mode, the cycle time of the trigger output unit operating in the indicated modes.	80	$\geq 32 + P_{WIDTH2}$		ns
t_{CYCNC1}	In cascade mode for TRIGX_CFG_1[6:4] = 100 or 101 (Neg. Periodic, Pos. periodic Output signals). Minimum cycle time for any trigger output unit operating in the indicated modes.	80	$\geq 32 + P_{WIDTH2}$		ns
t_{GAP23}	In cascade mode for TRIGX_CFG_1[6:4] = 010, and 011 (Neg. Pulse, Pos. Pulse Output signals): Minimum gap time required between end of period of first trigger output unit to beginning of output of 2nd trigger output unit.	80			ns
P_{WIDTH2}	In cascade mode, the minimum low or high pulse width of the trigger output unit.	8			ns
Trigger Output Unit Timing (Non-Cascade Mode)					
t_{CYCNC2}	In non-cascade mode, the minimum cycle time for any trigger output unit.	80	$\geq 32 + P_{WIDTH2}$		ns
t_{POGAP}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	32			ns
P_{WIDTH1}	In non-cascade mode, the minimum low or high pulse width of the trigger output unit.	8			ns
Timestamp Input Unit Timing					
IP_{HIGH}	Allowable high time of an incoming digital waveform on any GPIO pin.	24			ns
IP_{LOW}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	24			ns
IP_{CYC}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	48			ns

6.4.8 POWER-UP AND RESET TIMING

Figure 6-13 illustrates the power-up and reset timing requirements.

FIGURE 6-13: POWER-UP AND RESET TIMING

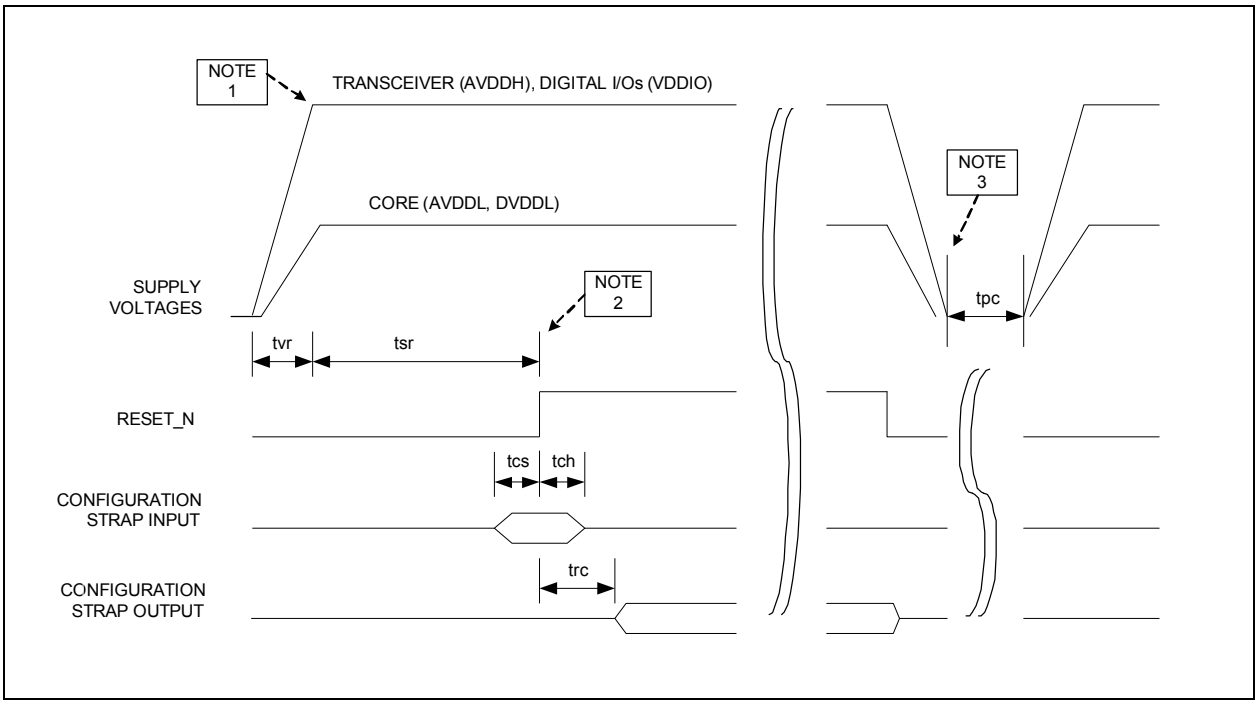


TABLE 6-12: POWER-UP AND RESET TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
tvr	Supply voltage rise time (must be monotonic)	200			µs
tsr	Stable supply voltages to de-assertion of reset	10			ms
tcs	Configuration strap input setup time	5			ns
tch	Configuration strap input hold time	5			ns
trc	De-assertion of reset to configuration strap pin output	6			ns
tpc	Supply voltages cycle off-to-on time	150			ms

Note 1: The recommended powering sequence is to bring up all voltages at the same time. However, if that cannot be attained, then the recommended power-up sequence is to power-up the transceiver (**AVDDH**) and digital I/Os (**VDDIO**) voltages before the low voltage core (**AVDDL** and **DVDDL**). There is no power sequence requirement between transceiver (**AVDDH**) and digital I/Os (**VDDIO**) power rails. The power-up waveforms should be monotonic for all supply voltages.

Note 2: After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting to program the device through any interface.

Note 3: The recommended power down sequence is to power down the low voltage core before powering down the transceiver and digital I/O voltages, or to have all supplies power down in unison.
Before the next power-up cycle, all supply voltages to the device should reach less than 0.4V and there should be a minimum wait time of 150ms from power-off to power-on.

6.5 Clock Specifications

A crystal or external clock source, such as an oscillator, is used to provide a 25MHz reference clock for the KSZ8567R. If an external clock source is used, the **XO** pin must be left floating. Since the **XI/XO** circuit is powered from **AVDDH**, the external clock source should also be powered from the same power rail. Figure 6-14 details the available connection methods. Table 6-13 details the recommended crystal specifications.

FIGURE 6-14: INPUT REFERENCE CLOCK CONNECTION OPTIONS

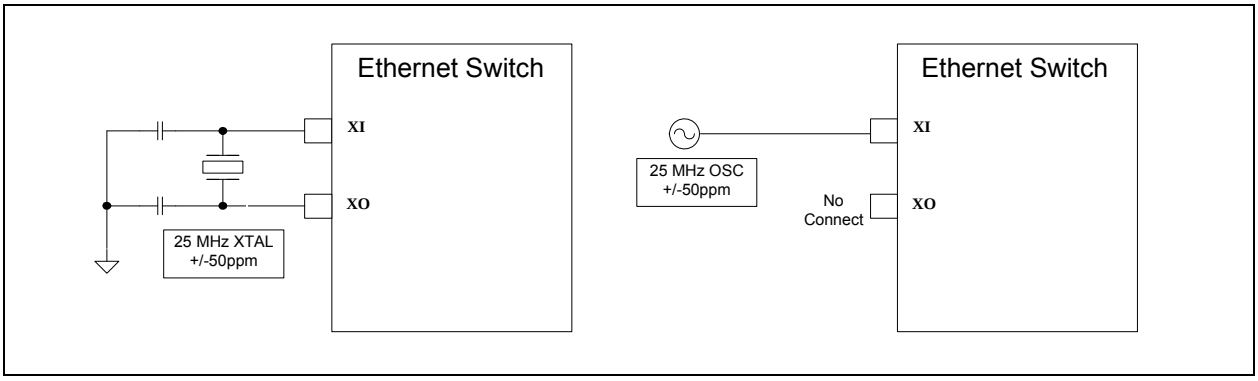


TABLE 6-13: REFERENCE CRYSTAL CHARACTERISTICS

Characteristic	Min	Typ	Max	Units
Oscillation Mode		Fundamental		
Frequency		25		MHz
Frequency tolerance			±50	ppm
Effective Series Resistance (ESR)			50	Ω
Total period jitter (peak-to-peak)			100	ps
Drive level			100	uW

7.0 DESIGN GUIDELINES

This section provides general design guidelines for the following:

- Reset Circuit Guidelines
- Magnetics Connection and Selection Guidelines

7.1 Reset Circuit Guidelines

Figure 7-1 illustrates the recommended reset circuit for powering up the KSZ8567R if reset is triggered by the power supply.

FIGURE 7-1: SIMPLE RESET CIRCUIT

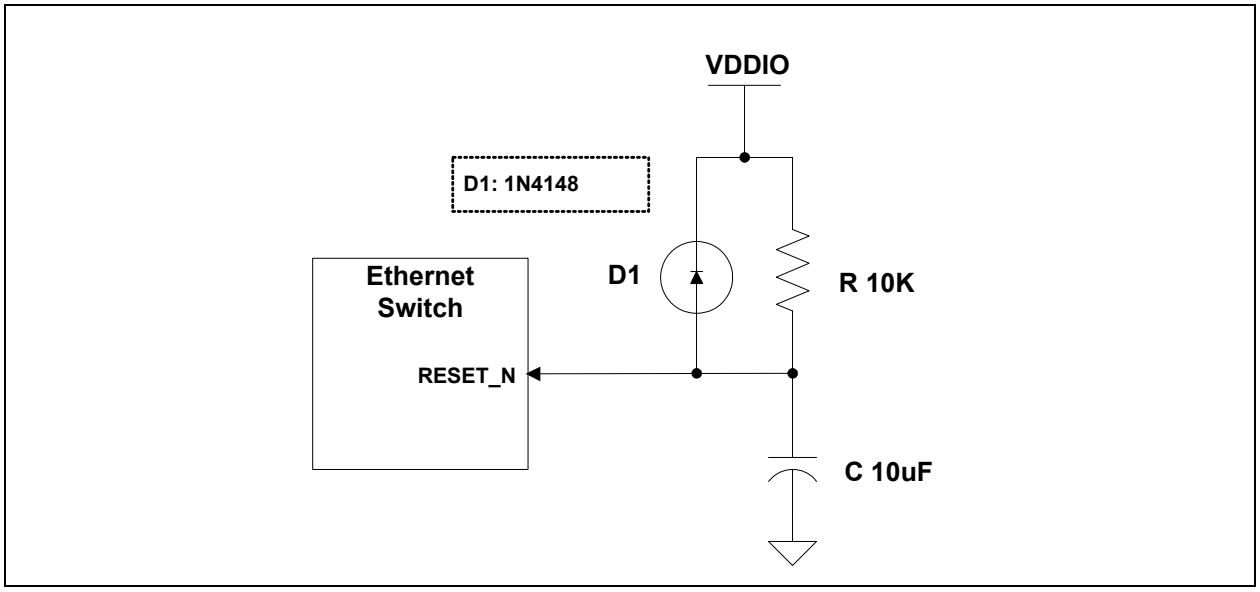
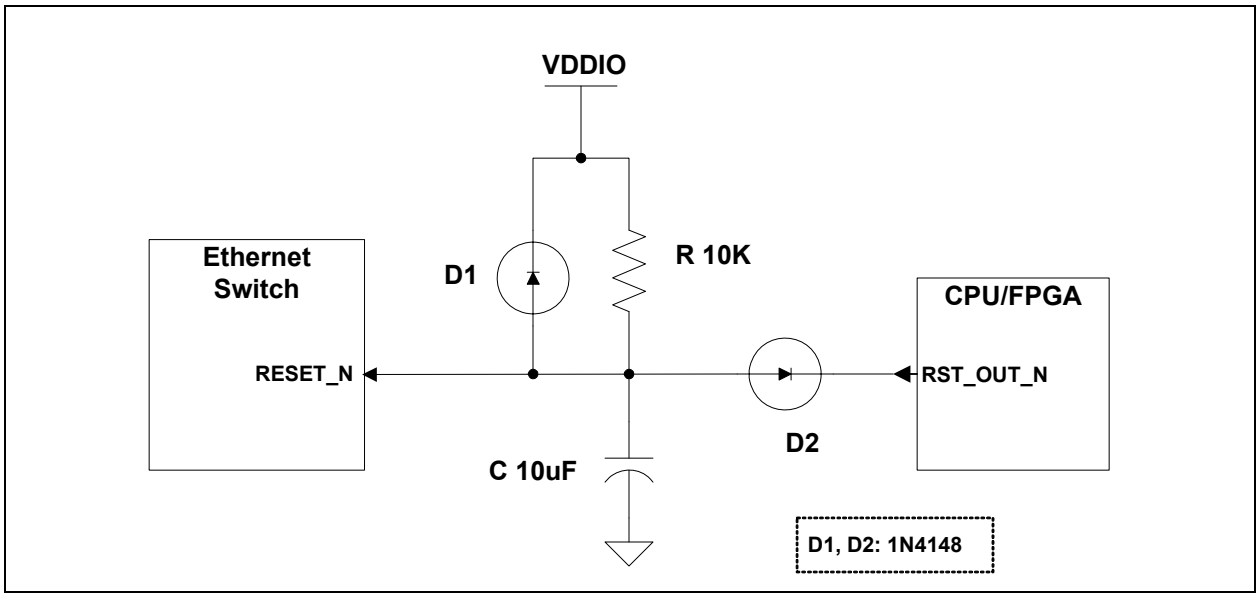


Figure 7-2 illustrates a reset circuit recommended for applications where reset is driven by another device, such as a CPU. At power-on reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8567R. The RST_OUT_N from the CPU provides a warm reset after power-up.

FIGURE 7-2: RESET CIRCUIT FOR CPU RESET INTERFACE



7.2 Magnetics Connection and Selection Guidelines

A 1:1 isolation transformer is required at the line interface. For designs exceeding FCC requirements, utilize one with integrated common-mode chokes. An optional auto-transformer stage following the chokes provides additional common-mode noise and signal attenuation.

The KSZ8567R PHY port design incorporates voltage-mode transmit drivers and on-chip terminations. With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the two differential pairs. Therefore, the two transformer center tap pins on the KSZ8567R chip side should not be connected to any power supply source on the board; rather, the center tap pins should be separated from one another and connected through separate 0.1µF common-mode capacitors to ground. Separation is required because the common-mode voltage could be different between the differential pairs, depending on the connected speed mode.

Figure 7-3 details a typical magnetic interface circuit for the KSZ8567R PHY port.

FIGURE 7-3: TYPICAL MAGNETIC INTERFACE CIRCUIT

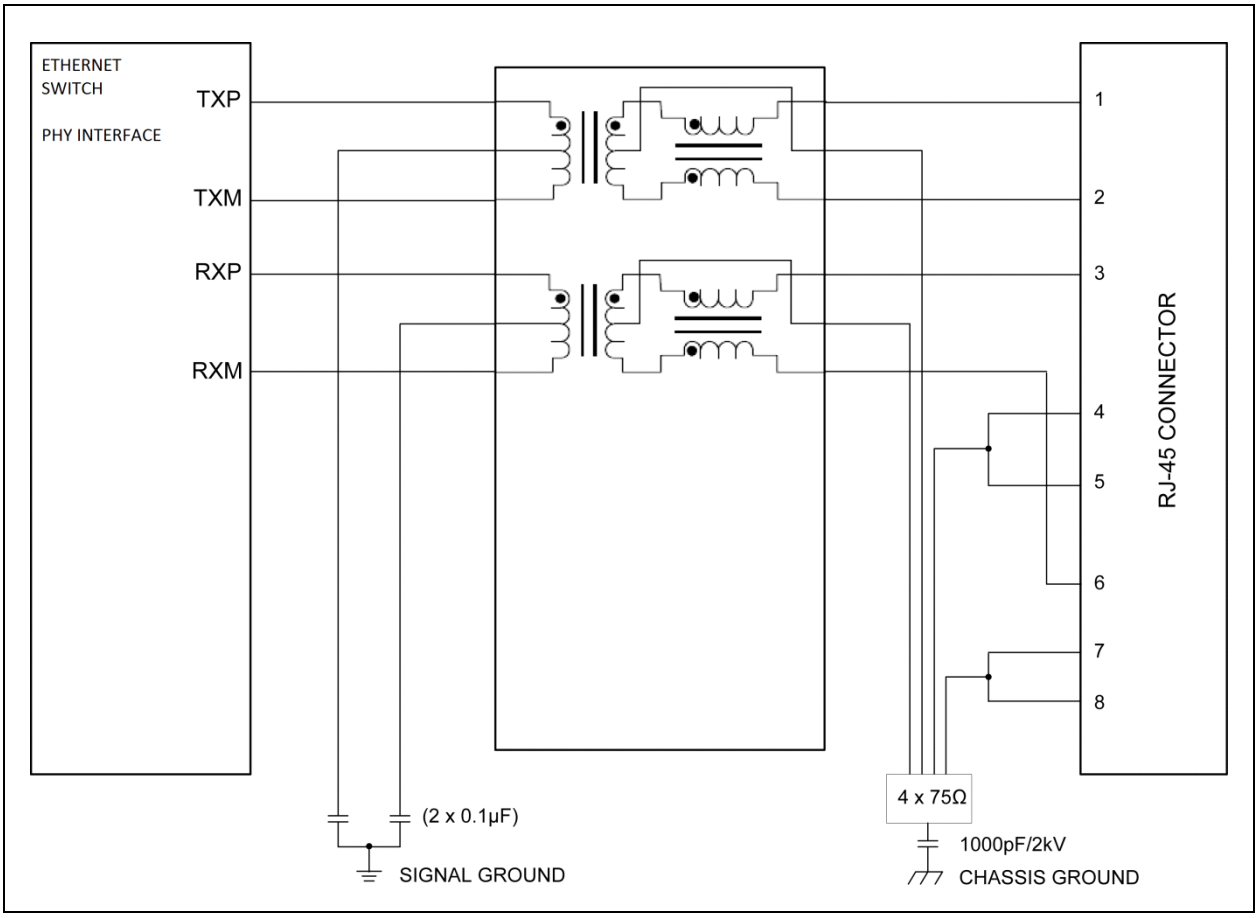


Table 7-1 provides a list of recommended magnetic characteristics.

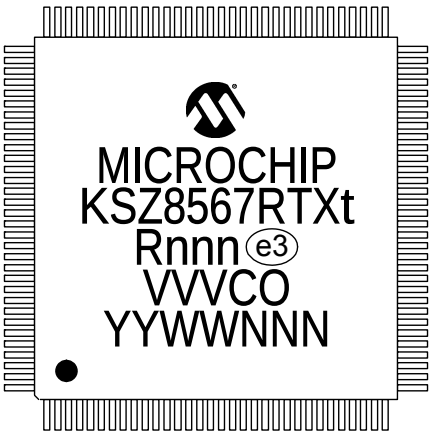
TABLE 7-1: MAGNETICS SELECTION CRITERIA

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350µH	100mV, 100KHz, 8mA
Insertion loss (typ.)	1.0dB	100KHz to 100MHz
HIPOT (min.)	1500vrms	

8.0 PACKAGE INFORMATION

8.1 Package Marking Information

128-TQFP-EP



Legend:	t	Temperature range designator (I = industrial, V = Extended)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	VVV	Plant assembly
	CO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

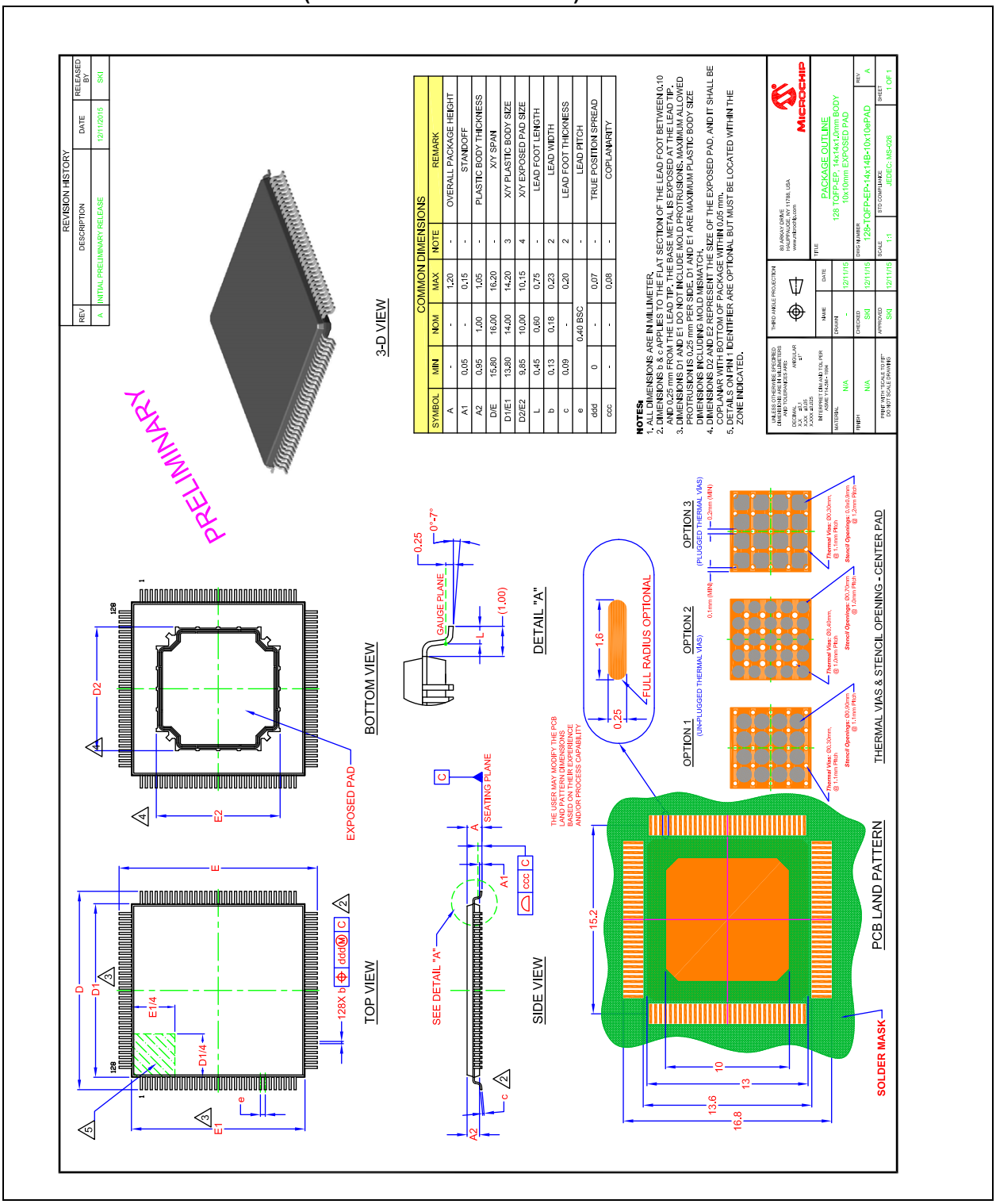
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8.2 Package Drawings

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 8-1: PACKAGE (DRAWING & DIMENSIONS)



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002328B (03-10-17)	Section 4.1.10, "Remote PHY Loopback," on page 22	Added new section.
	Section 4.4.5.1, "Two Rate Three Color Marker," on page 34	Added new section.
	Section 4.4.5.2, "Weighted Random Early Detection (WRED)," on page 34	Updated section with additional information.
	Section 4.11.3, "MII Management (MIIM) Interface," on page 57, Section 4.11.3.1, "Standard MIIM Registers (Direct)", Section 4.11.3.2, "MDIO Manageable Device (MMD) Registers (Indirect)"	Added additional information to end of section. Added new subsections on Standard MIIM and MMD registers.
	Section 5.4, "MDIO Manageable Device (MMD) Registers (Indirect)," on page 195	Added new section.
	Section 5.2.7.8, "Port Police Queue Rate Register," on page 169 through Section 5.2.7.14, "Port WRED Queue Performance Monitor Control Register," on page 171	Added new register definitions.
	Section 6.4.1, "RGMII Timing," on page 201	Updated RGMII timing diagrams and data.
	Table 1-2, “Buffer Types,” on page 6, Table 3-2, “Pin Descriptions,” on page 11, Table 6-1, “Electrical Characteristics,” on page 198	Updated/Clarified pin buffer type information.
DS00002328A (01-13-17)	Initial Document Release	

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PART NO.	XX	X	[XX](1)
Device	Package	Temp. Range	Tape & Reel Option

Device:	KSZ8567R = 7-Port Switch with 2 RGMII/MII/RMII Interfaces	
Package:	TX	= 128-pin TQFP-EP
Temperature Range:	I	= -40°C to +85°C (Industrial)
	V	= -40°C to +105°C (Extended)
Tape and Reel Option:	Blank	= Standard packaging (tray)
	-TR	= Tape and Reel (Note 1)

Examples:

a) KSZ8567RTXI
128-pin TQFP-EP package,
Industrial temperature,
Standard packaging

b) KSZ8567RTXV-TR
128-pin TQFP-EP package,
Extended temperature,
Tape and reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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